

Technische Universität Graz

# Physics of Semiconductor Devices

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#### Technische Universität Graz

# Physics of Semiconductor Devices

- Diodes, solid state lasers, transistors
- Computing, communications
- Controllers: vacuum cleaners, coffee makers, etc.
- Transportation, autonomous driving, electric cars
- Efficient lighting, solar cells, displays
- Lasers



#### http://lampz.tugraz.at/~hadley/psd/outline/outline.php



#### **PHT.301 Physics of Semiconductor Devices**

Home	
Outline	
Introduction	
Electrons in cryst	als
Intrinsic Semicon	ductors
Extrinsic Semicor	nductors
Transport	
pn junctions	
Contacts	
JFETs/MESFETs	
MOSFETs	
Bipolar transistor	S
Opto-electronics	
Lectures	
Books	
Exam questions	
Mathmatical expr	essions
TUG students	
Student projects	

#### Outline

- Introduction
  - Semiconductors, transistors, and the electronics industry
- Semiconductor crystals
  - Energy bands
     W
    - Crystal structure
    - Bravais lattice W
    - Miller indices
    - Examples of crystal structures
      - silicon, GaN (wurzite), SiC 4H, ZnO (wurzite), diamond
      - simple cubic, fcc, bcc, hcp, zincblende
    - Wave and particle nature of electrons
    - k-space
    - Density of states W Some examples: Al fcc, Au fcc, Cu fcc, Pt fcc, W bcc, Si diamond, Grap
    - Pauli exclusion principle
    - Fermi function
    - Fermi energy W
    - Metals, semiconductors, and insulators
    - Metal band structure
    - Semiconductor band structure
  - Absorption and emission of photons
  - o Direct and indirect band gaps W
- Intrinsic semiconductors
  - Conduction band
  - Valence band
  - Effective mass
  - o Holes W
  - o Boltzmann approximation
  - o Law of mass action W
  - ∘ Fermi energy of an intrinsic semiconductor ► EN 2:36
  - o Intrinsic semiconductors with a split-off band



#### **Technische Universität Graz**

## Examination

1 hour written exam

One page of handwritten notes

1 Contribution to improve the course

Chapter summaries

Solutions to exam questions

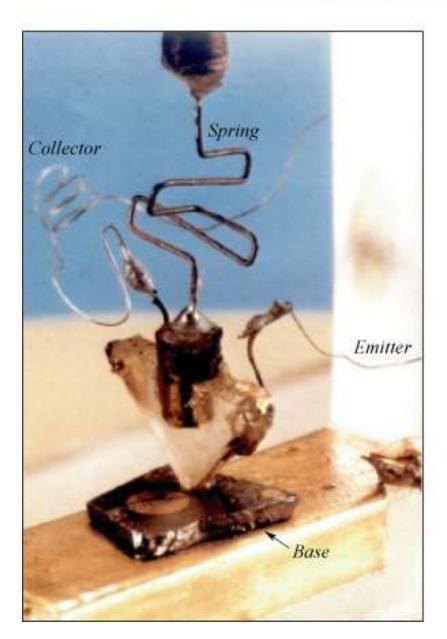
**Simulations** 

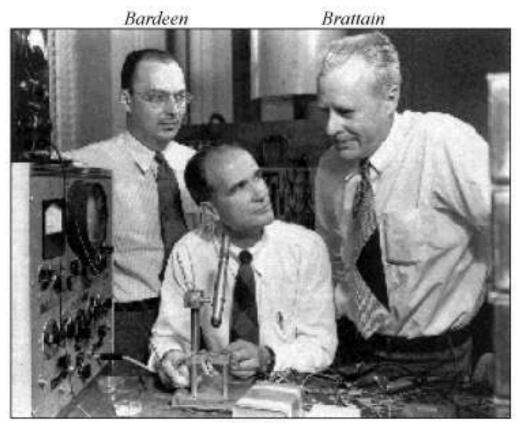
Videos

Oral exam

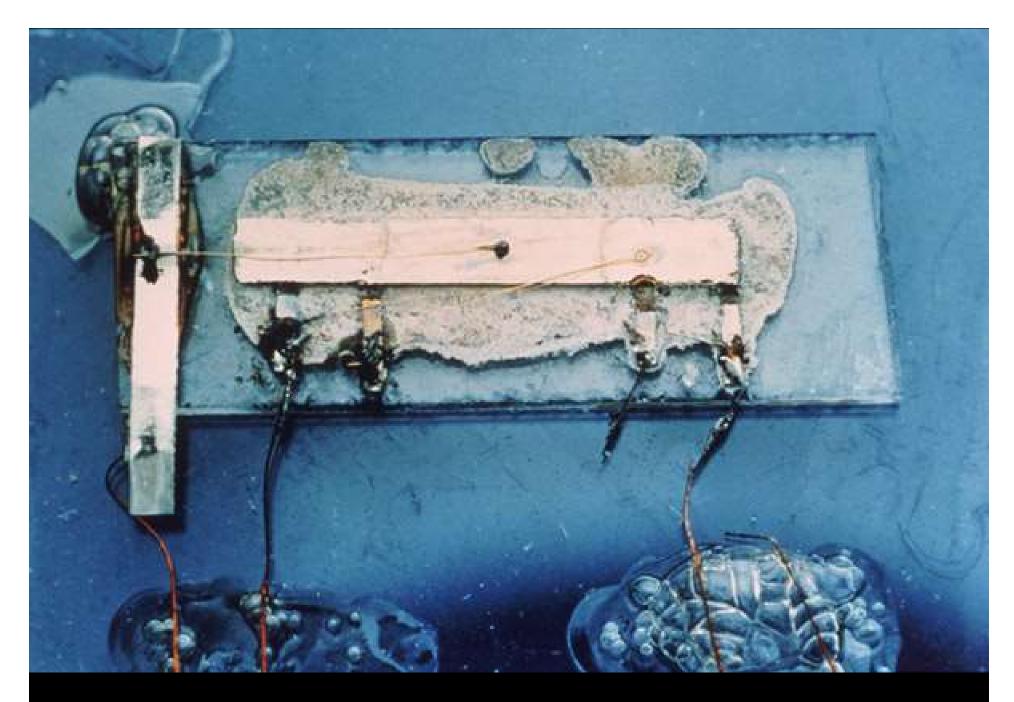
### The first point contact transistor

William Shockley, John Bardeen, and Walter Brattain Bell Laboratories, Murray Hill, New Jersey (1947)





Shockley

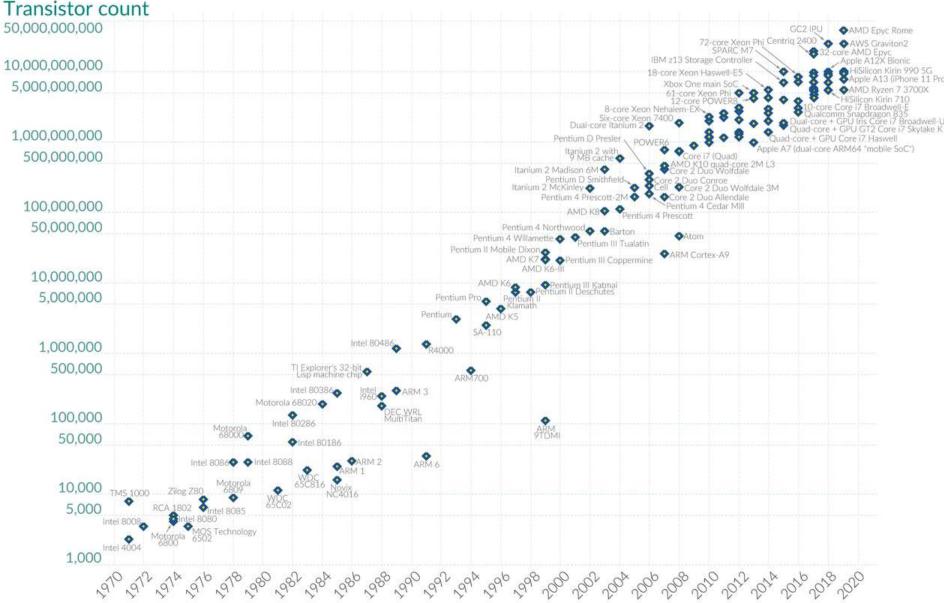


Jack Kilby's first integrated circuit 1958

#### Moore's Law: The number of transistors on microchips doubles every two years Our World



Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.



Data source: Wikipedia (wikipedia.org/wiki/Transistor count)

Year in which the microchip was first introduced

OurWorldinData.org - Research and data to make progress against the world's largest problems.

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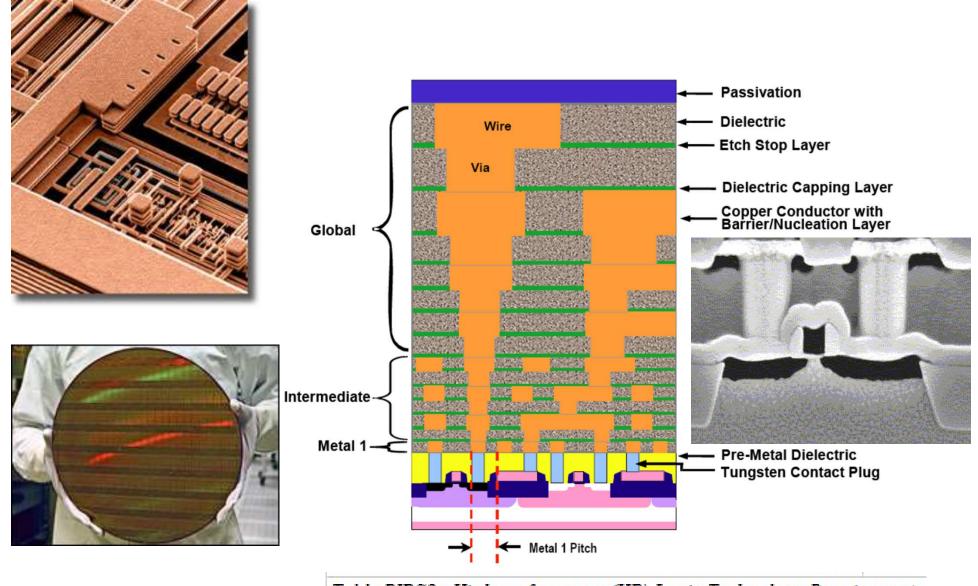
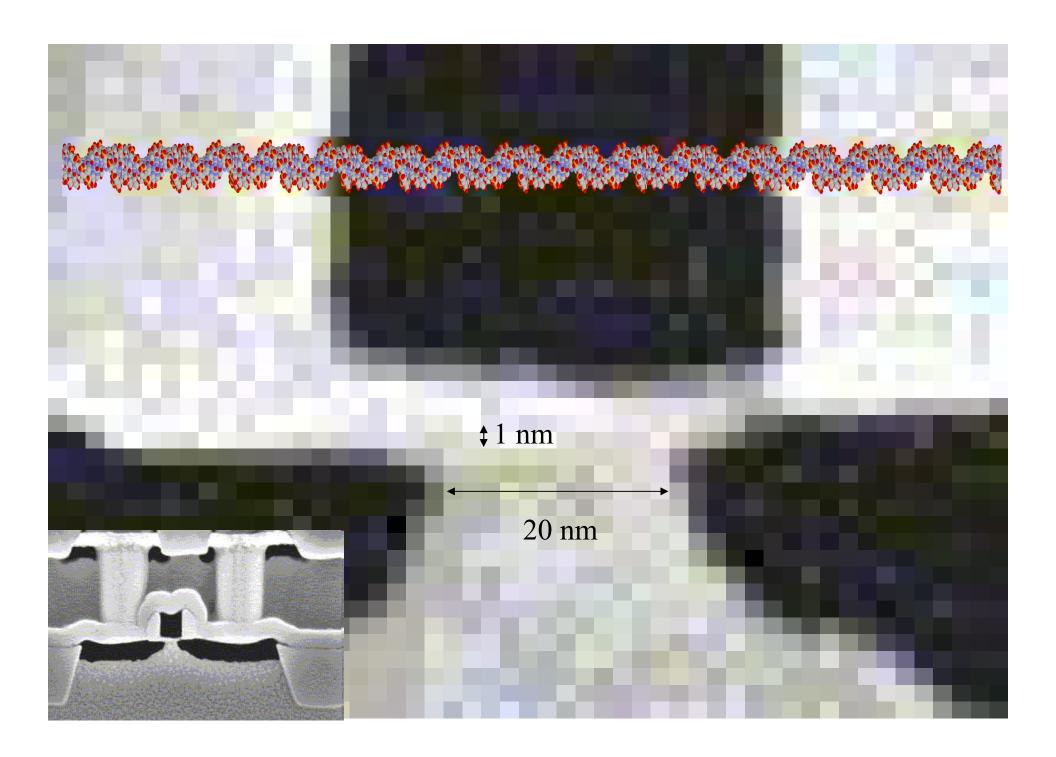


Table PIDS2a High-performance (HP) Logic Technology Requirements

				. 2		73				23						
	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
node	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
metal 1/2 pitch	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
gate length	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1
	40.0	444	42.4	422	44.4	40.2	0.0	0.5	7.0	7.0	C 4	r 0	F 4	4.0	4.5	4.4





#### https://irds.ieee.org

#### INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS TM





INTERNATIONAL
ROADMAP
FOR
DEVICES AND SYSTEMS

2017 EDITION

EXECUTIVE SUMMARY

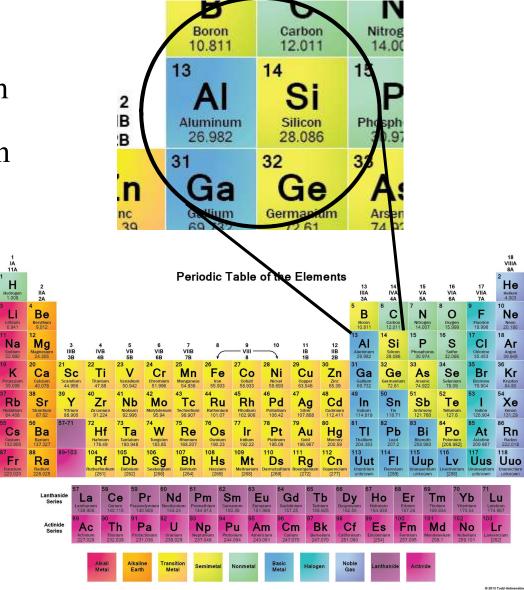
- 1. Application Benchmarking (AB)
- 2. Systems and Architectures (SA)
- 3. Outside System Connectivity (OSC)
- 4. More Moore (MM)
- 5. Beyond CMOS (BC)
- 6. Packaging Integration (PI)
- 7. Factory Integration (FI)
- 8. Lithography (L)
- 9. Emerging Research Materials (ERM)
- 10. Yield Enhancement (YE)
- 11. Metrology (M)
- 12. Environment, Safety, Health (ESH/S), and Sustainability

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"4.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET	finFET	LGAA	LGAA	LGAA	VGAA, LGAA	VGAA, LGAA
Logic device structure options	FDSOI	LGAA	finFET	VGAA	VGAA	3DVLSI	3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
	FinFET	FINEY	Lateral Nanowine	Lateral Nanowire	Lateral Nanowire	Vertical Nanowire	Vertical Nanowire
	45-47						
							-
	FD-501	Lateral Nanowine	FINFET	Vertical Nanowire	Vertical Nanowire	Monolitric 3D	MonoRhic 3D
	AND DESCRIPTION OF THE PERSON	(E19)	A Ch	-		100 to 100 100 100 100 100 100 100 100 100 10	
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LANGE BETWEE CRAIMS BUT ES	441	No. of	NAME OF TAXABLE PARTY.	-	Distance	THE REAL PROPERTY.	Mark Control
LOGIC DEVICE GROUND RULES	40.0	440	40.0		7.0	7.0	7.0
MPU/SoC Metalx ½ Pitch (nm)[1,2]	18.0	14.0	12.0	10.5	7.0	7.0	7.0
MPU/SoC Metal0/1 1/2 Pitch (nm)	18.0	14.0	12.0	18.5	7.0	7.0	7.0
Contacted poly half pitch (nm)	27.0	24.0	21.0	18.0	16.0	16.0	16.0
La: Physical Gate Length for HP Logic (nm) [3]	20	18	16	14	12	12	12
L <sub>a</sub> : Physical Gate Length for LP Logic (nm)	22	20	18	16	14	14	14
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	8	7	6	5	5	5	5
Contact CD (nm) - finFET, LGAA	18	16	14	12	10		
Contact CD (nm) - VGAA						12	12
Device architecture key ground rules	092820		4				
FinFET Fin Half-pitch (nm)	16.0	14.0					
FinFET Fin Width (nm)	8.0	7.0					
FinFET Fin Height (nm)	45	50					
Footprint drive efficiency - finFET	3.06	3.82					
Lateral GAA lateral half-pitch (nm)			12.0	10.5	9.0	<u> </u>	
Lateral GAA vertical half-pitch (nm)			8.0	8.0	8.0		
Lateral GAA (nanosheet) thickness (nm)			5.0	5.0	5.0		
Lateral GAA (nanosheet) minimum width (nm)			7.0	7.0	6.0		
Number of vertically stacked nanosheets			3	4	5		
Device height (nm)			47	63	79		
Footprint drive efficiency - lateral GAA			3.00	4.57	6.11		7.0
Vertical GAA lateral half-pitch (nm)						7.0	7.0
Vertical GAA width (nm)						6.0	6.0
Contact-gate enclosure (nm)						2.0	2.0
Footprint drive efficiency - vertical GAA	00.5	407.7	70.0	20.0		1.7	1.7
Defice effective width (nm)	98.0	107.0	72.0	96.0	110.0	24.0	24.0
Device lateral half pitch (nm)	16.0	14.0	12.0	10.5	9.0	7.0	7.0
Device height (nm)	45.0	50.0	47.0	63.0	79.0	24.0	24.0
Minimum device width (fin, nanosheet) or diameter (nm)	8.0	7.0	7.0	7.0	6.0	6.0	6.0

### Conductivity

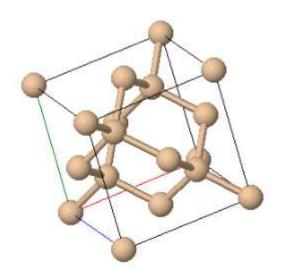
Al:  $\sigma = 3.5 \times 10^7 \text{ } 1/\Omega \cdot \text{m}$ 

Si:  $\sigma = 4.3 \times 10^{-4} \text{ 1/}\Omega \cdot \text{m}$ 



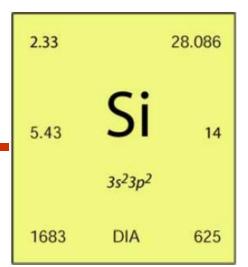
## Silicon

- Important semiconducting material
- 2nd most common element on earths crust (rocks, sand, glass, concrete)
- Often doped with other elements
- Oxide SiO<sub>2</sub> is a good insulator





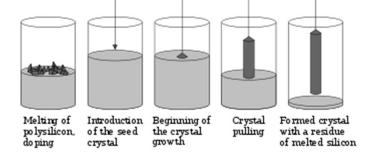
silicon crystal = diamond crystal structure



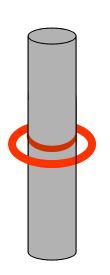
## Silicon

Large (2 m) single crystals are grown

Czochralski process



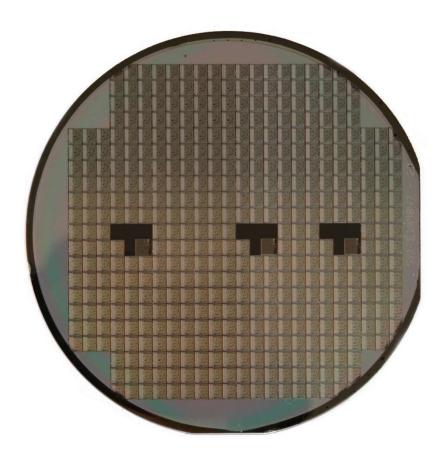




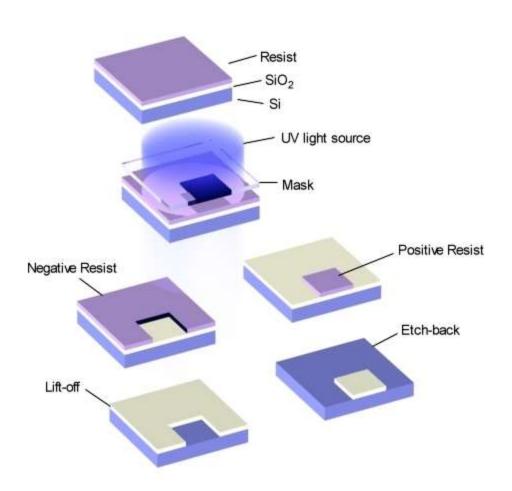
Float zone

# Silicon wafers

 $50 \ \mu m$  -  $0.5 \ mm$  thick



# Photolithography

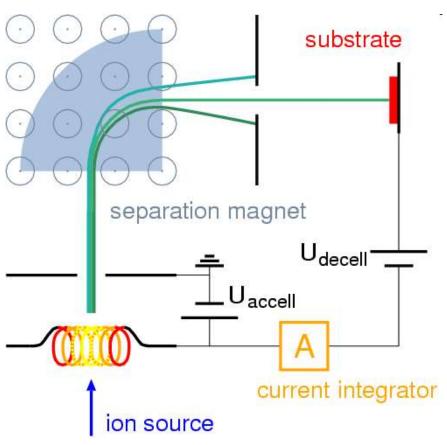


http://britneyspears.ac/physics/fabrication/photolithography.htm

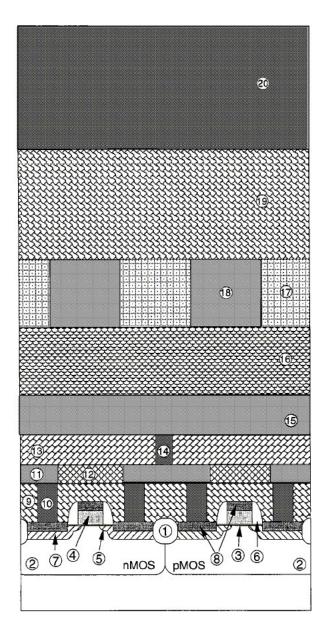
http://cleanroom.byu.edu/lithography.parts/Lithography.html

# Ion implantation

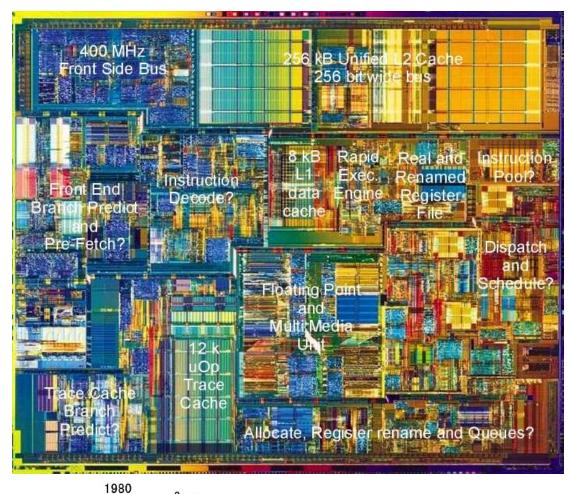


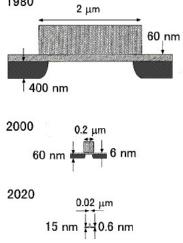


Implant at 7° to avoid channeling



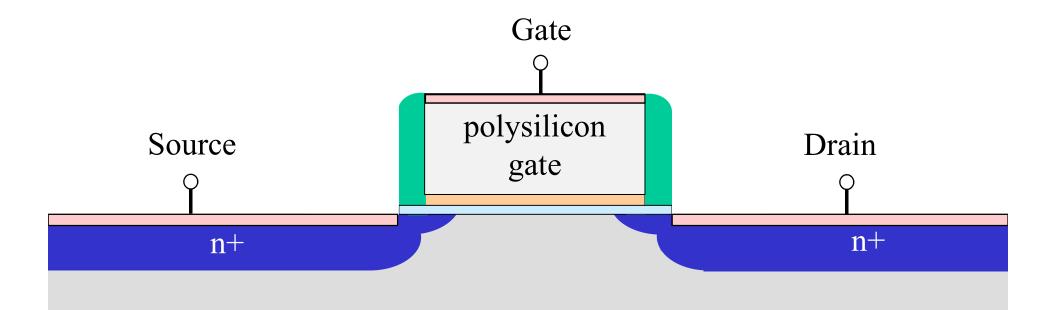
 $\label{eq:Fig.2} \textbf{Fig. 2} \quad \text{Schematic cross section of present CMOS FETs with multilayered wiring.}$ 





## MOSFET

Metal Oxide Semiconductor Field Effect Transistor



functions as a switch ~ 1 billion /chip

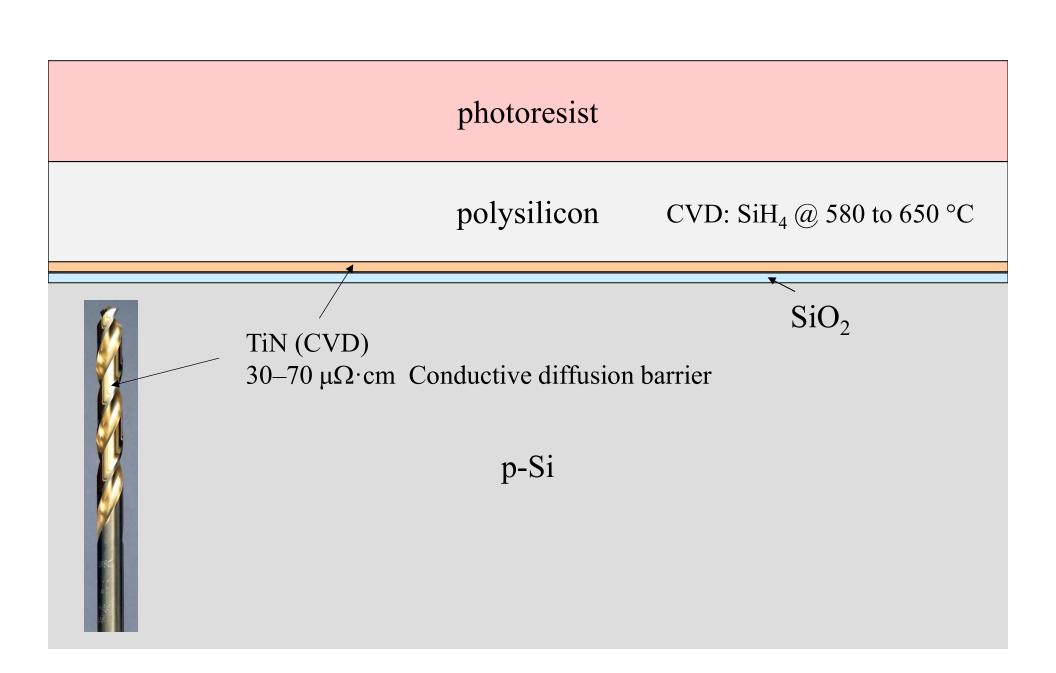
# Self-aligned fabrication

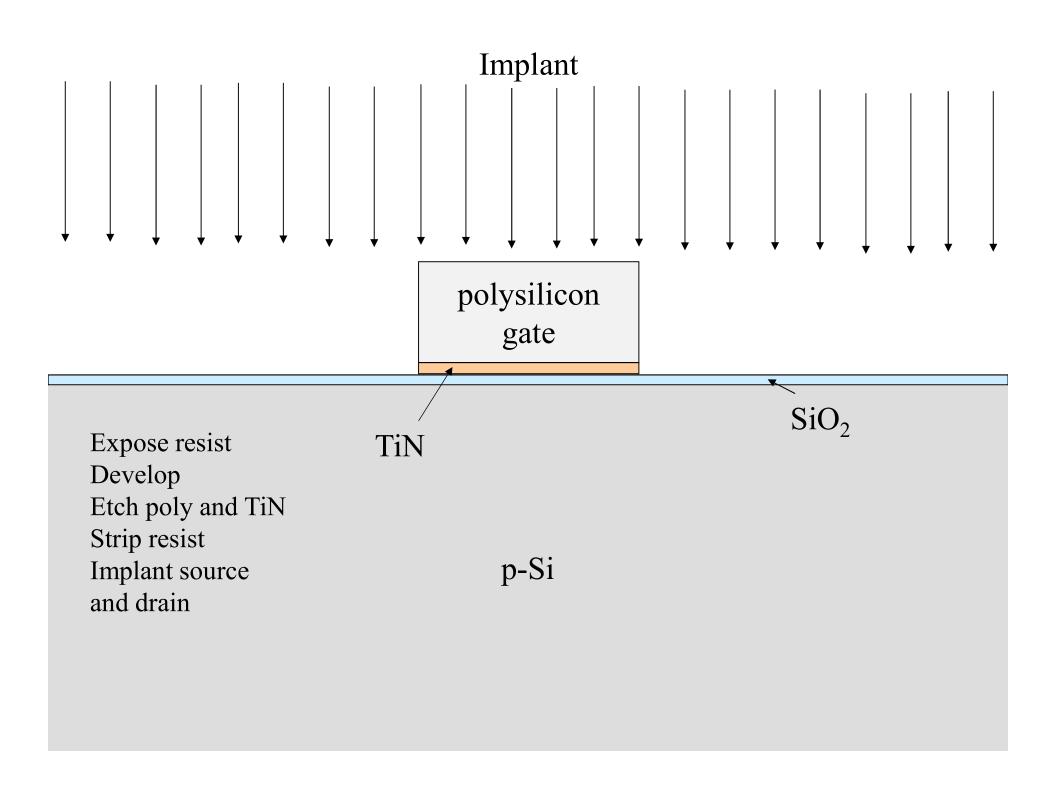
p-Si 100 wafer

## Dry oxidation

SiO<sub>2</sub> gate oxide

p-Si





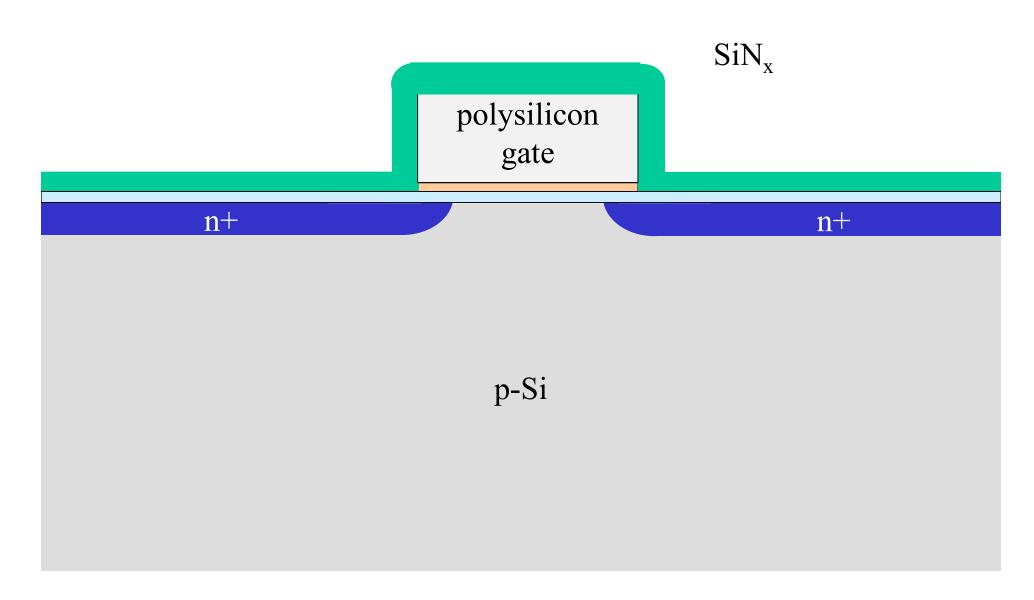
# Self-aligned fabrication

polysilicon gate

n+ n+

# Spacer

 $PECVD SiN_x$ 



# Spacer

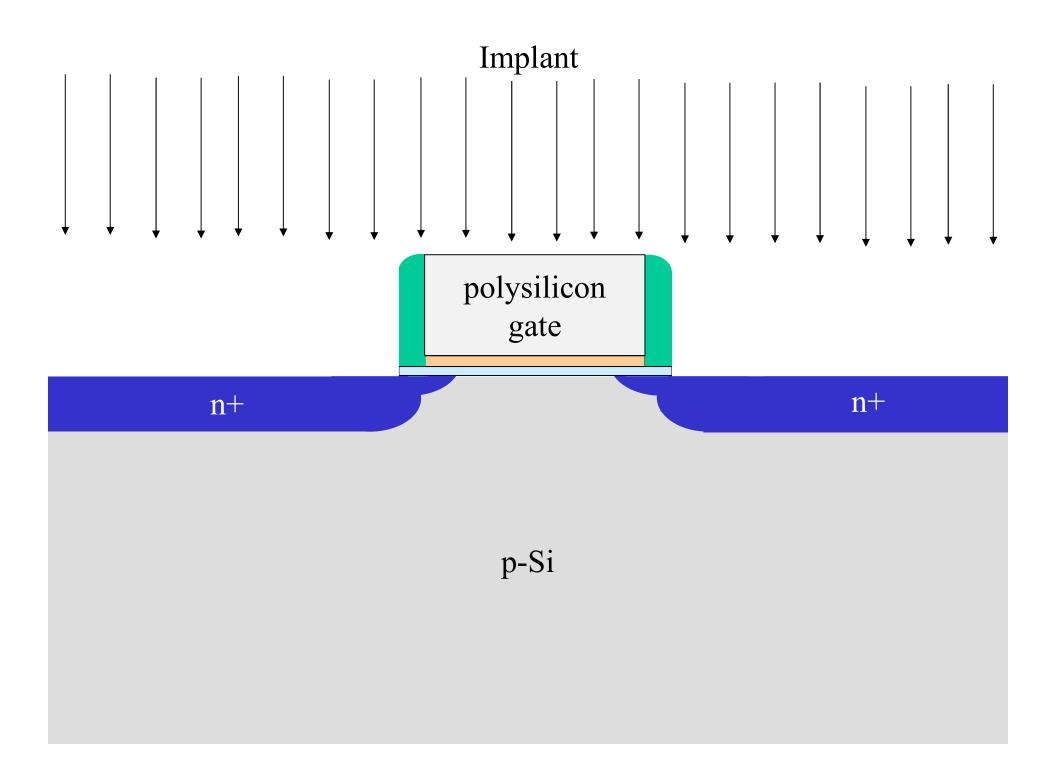
Etch back to leave only sidewalls

 $SiN_x$ 

polysilicon gate

n+

p-Si



# Salicide (Self-aligned silicide)

