

Simulating Hybrid Circuits of Single-Electron Transistors and Field-Effect Transistors

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An exact model for a single-electron transistor was developed within the circuit simulation package SPICE. This model uses the orthodox theory of single-electron tunneling and determines the average current through the transistor as a function of the bias voltage, the gate voltage, and the temperature. Circuits including single-electron transistors, field-effect transistors (FETs), and operational amplifiers were then simulated. In these circuits, the single-electron transistors provide the charge sensitivity while the FETs tune the background charges, provide gain, and provide low output impedance. [DOI: 10.1143/JJAP.42.6467]

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1. Introduction

Single-electron transistors (SETs) are used to perform sensitive charge measurements and are widely discussed as possible components of dense integrated circuits.¹⁾ These devices are attractive for applications in integrated circuits because they can be very small and they dissipate little power. However, SETs have low gain, high output impedances, and are sensitive to random background charges. This makes it unlikely that single-electron transistors would ever replace field-effect transistors (FETs) in applications where large voltage gain or low output impedance is necessary. The most promising applications for SETs are charge sensing applications such as the readout of few electron memories,²⁾ the readout of charge-coupled devices, and precision charge measurements in metrology.³⁾ In these applications, field-effect transistors are used to buffer the high output impedance of SETs and to automatically tune the background charges. Here we present a SPICE model for a single-electron transistor that can be used to perform simulations of circuits where single-electron transistors are combined with any other circuit elements.

Several very good single-electron circuit simulation programs already exist. Notable among these are SIMON⁴⁾ and MOSES.⁵⁾ However, these simulation programs cannot include many standard electronic components such as diodes and transistors. We have chosen to model the SET circuits using SPICE⁶⁾ because it is so widely used to analyze electronic circuits. Extensive libraries of digital and analog circuit elements exist for SPICE. Other SPICE models for single-electron transistors also exist. These models are either phenomenological models,⁷⁾ simplifications of the orthodox theory of single-electron tunneling,^{8–10)} or they use extensions of SPICE that are not generic to all versions of SPICE.¹¹⁾ Here we describe an implementation of the full orthodox theory that uses only the capabilities in publicly available versions of SPICE.¹²⁾ The model uses a stationary master equation approach that is suitable for quickly evaluating small circuits that combine SETs and other standard circuit elements. The model presented here is not limited to single-electron transistors with tunnel junctions that have equal resistances and can be extended to include an arbitrary number of charge states enabling SET simulations for arbitrarily high temperatures and bias voltages.

In §2, the orthodox theory calculation is sketched and the implementation of this theory in a SPICE model is discussed. The model is then validated by comparing the current through a single-electron transistor predicted by the SPICE-SET model with the simulations of a conventional Monte-Carlo circuit simulator. In §3, SPICE simulations of circuits consisting of only SETs are described. In particular, simulations of an inverter circuit and a ring oscillator are discussed. In §4, simulations of hybrid circuits involving SETs, FETs, and operational amplifiers are described. In the simulations, field effect transistors are used to current bias SETs, to buffer the high output impedance, and to tune the background charges. While this SPICE model can be used to simulate circuits where single-electron transistors are combined with any other circuit elements, we only consider circuits that combine SETs and FETs since these are the most interesting for charge sensing applications.

2. The Model

Figure 1 shows a schematic of a SET indicating the two tunnel junctions. In the model described here, two gates are coupled to the island. This is because many circuit applications require SETs with two gates. A voltage source is attached to each electrode (the source, the drain, and the two gates). In addition to the two gates, a stray capacitance C_0 to ground and a background charge Q_0 are included in the model.

To determine the average current that flows through the transistor, first the voltages of the island for the relevant charge states must be calculated. Simple electrostatics will show that the voltage of the island when a charge of ne is present on the island is,

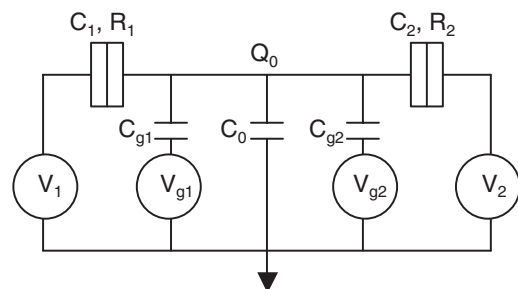


Fig. 1. A schematic diagram of a single-electron transistor showing the two tunnel junctions, two gates, the stray capacitance C_0 , and the background charge Q_0 .

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$$V(n) = (ne + Q_0 + C_1 V_1 + C_2 V_2 + C_{g1} V_{g1} + C_{g2} V_{g2}) / C_\Sigma. \quad (2.1)$$

Here e is the positive elementary charge, n is an integer that specifies the number of elementary charges that have been added to the island, $C_\Sigma = C_1 + C_2 + C_{g1} + C_{g2} + C_0$ is the total capacitance of the island of the transistor, and the other quantities are defined in Fig. 1. The energy it takes to move an infinitesimally small charge dq from ground at a potential $V = 0$ to the island is Vdq . As soon as a charge is added to the island, the voltage of the island changes. By integrating Vdq from 0 to e one can show that the electrostatic energy needed to add a charge e to the island is,

$$eV(n) + e^2 / (2C_\Sigma). \quad (2.2)$$

The change in energy when a charge e tunnels from a lead at voltage V_i to the island is thus,

$$\Delta E_i = -eV_i + eV(n) + e^2 / (2C_\Sigma). \quad (2.3)$$

When a charge of e tunnels from the island to a lead, the signs of the first two terms in eq. (2.3) are reversed. The change in energy can be used to calculate the tunnel rate which is given by the expression,

$$\Gamma_i = \frac{\Delta E_i}{e^2 R_i (\exp(\Delta E_i / k_B T) - 1)}, \quad (2.4)$$

where R_i is the tunnel resistance, T is the temperature and k_B is Boltzmann's constant. There are four possible single-electron tunneling events for a SET. A charge e can tunnel left through tunnel junction 1 (Γ_{1L}), one can tunnel right through tunnel junction 1 (Γ_{1R}), one can tunnel left through tunnel junction 2 (Γ_{2L}), or one can tunnel right through tunnel junction 2 (Γ_{2R}). Higher order tunnel events where two electrons tunnel simultaneously are not considered in this model.

Once the rates for all the relevant charge states have been determined, the probabilities that the charge states are occupied can be determined from the recursion relation,

$$P(n) = P(n-1) \left(\frac{\Gamma_{2L}(n-1) + \Gamma_{1R}(n-1)}{\Gamma_{2R}(n) + \Gamma_{1L}(n)} \right). \quad (2.5)$$

The average current flowing through the transistor in the direction from tunnel junction 1 to tunnel junction 2 is,

$$I = \sum_n eP(n)(\Gamma_{1R}(n) - \Gamma_{1L}(n)), \quad (2.6)$$

and the average voltage of the island is,

$$V = \sum_n P(n)V(n). \quad (2.7)$$

To efficiently calculate the current and voltage, first the charge state n that has the highest probability to be occupied should be determined. This charge state can be estimated using eq. (2.5). The most probable charge state is,

$$n_{\text{opt}} = -(Q_0 + C_1 V_1 + C_2 V_2 + C_{g1} V_{g1} + C_{g2} V_{g2}) / e + \frac{C_\Sigma}{e} \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}. \quad (2.8)$$

Equations (2.1)–(2.8) were implemented in SPICE to calculate the values for the voltage source E1 and the current source G1 in the SPICE-SET model depicted in Fig. 2. The

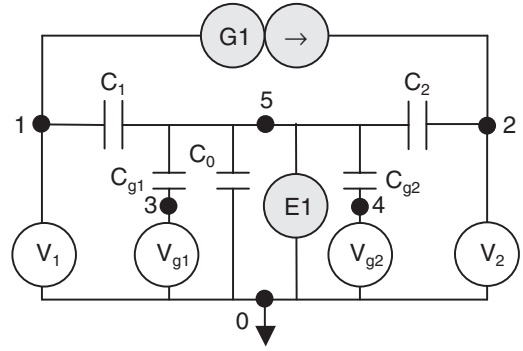


Fig. 2. The model of a SET in SPICE. The white voltage sources are external to the SET model and the gray sources are internal to the model. E1 is a voltage source that fixes the voltage of the island of the SET (node 5) using eq. (2.7) and G1 is a current source that specifies the source-drain current using eq. (2.6).

exact details and the complete source code of the model and for all the simulations described in this paper can be found online on our group's Internet site.

The model can handle arbitrarily large gate voltages. Depending on the number of charge states implemented in the model, it can also handle arbitrarily high bias voltages and temperatures. The simulation time is linearly dependent on this number of charge states. The simulations described here were performed with a SPICE-SET model that includes eleven charge states around the most probable charge state. This is sufficient to perform room temperature simulations of transistors with a total capacitance of a few attoFarads. It is straightforward to extend this model to include more charge states as outlined in the source code on the Internet. By comparing the charging energy with the electron energies that are provided by the temperature and the expected maximum voltage difference ΔV_{max} between source and drain, the number of charge states necessary can be estimated by,

$$n \approx \frac{2C_\Sigma}{e^2} (e\Delta V_{\text{max}} + 7k_B T). \quad (2.9)$$

Here we have chosen to consider only electrons with a thermal energy of less than $7k_B T$ which leaves us with an accuracy of about e^{-7} for the tunnel rates, ie. the accuracy is in the 0.1% range.

Figure 3 compares the simulations of a single-electron transistor using the SPICE-SET model (black lines) with the ones using a conventional Monte-Carlo simulation program (gray lines). For the Monte-Carlo simulations we used SIMON and we chose simulation parameters that resulted in approximately the same calculation time on a Pentium computer as the SPICE-SET simulation. As it clearly can be seen, the simulations give identical results except for some wiggles in the Monte-Carlo simulation lines which are due to the stochastic character of the Monte-Carlo algorithm.

In Fig. 3(a), the current–voltage characteristics are plotted for a number of gate voltages. Figure 3(b) shows the current through a SET as a function of the gate voltage for a number of bias voltages. These periodic current oscillations are known as Coulomb oscillations. If the thermal fluctuations ($\approx k_B T$) are larger than the energy it takes to add an electron to the island, the Coulomb blockade is washed out. This is demonstrated in Fig. 3(c) where the current–voltage charac-

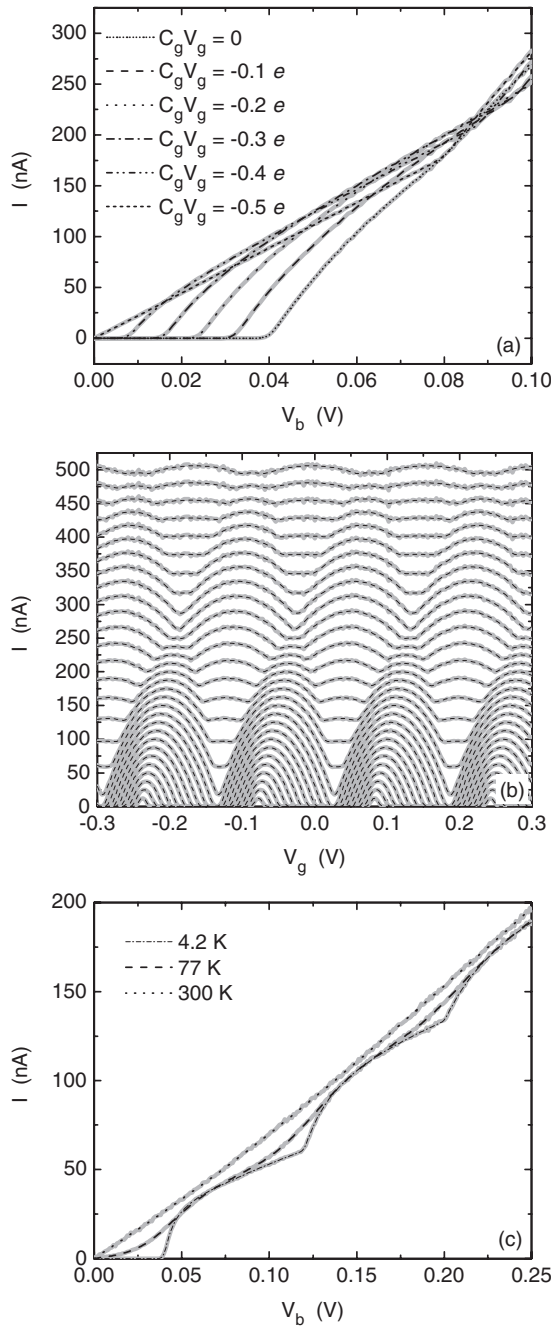


Fig. 3. Comparison of the single-electron transistor simulations performed with the SPICE-SET model (black lines) with the ones performed with a conventional Monte-Carlo simulation program (gray lines). In all three simulations the parameters used were: $C_1 = C_2 = 1$ aF, $C_g = 1$ aF, $C_{g2} = 0$, $C_0 = 0$, $V_1 = 0$, $V_{g2} = 0$, $Q_0 = 0$. (a) The current through the SET transistor is plotted as function of the bias voltage for six gate voltages, $T = 4.2$ K, $R_1 = R_2 = 100$ k Ω . (b) The current through the SET transistor is plotted against the gate voltage for bias voltages $V_2 = 5$ mV to 150 mV in steps of 5 mV, $T = 4.2$ K, $R_1 = R_2 = 100$ k Ω . (c) Current-voltage characteristics are plotted for three different temperatures, $V_{g1} = 0$, $R_1 = 100$ k Ω , $R_2 = 1$ M Ω .

teristic is plotted for three different temperatures. In this simulation, a Coulomb staircase is clearly seen in the low temperature simulation. A Coulomb staircase is observed if the two tunnel junctions have greatly different resistances. The simulations in Fig. 3 were done for junction capacitances of $C_1 = C_2 = 1$ aF. These are approximately the smallest junction capacitances that have been reproducibly obtained experimentally. Junction capacitances of this magnitude

were obtained by Pashkin *et al.*¹³⁾ using electron-beam lithography to define a 2 nm aluminum island. This was also achieved by Park *et al.*¹⁴⁾ by using a C_{60} molecule as the conducting island. Ono *et al.*¹⁵⁾ achieved such small junction capacitances in silicon by using pattern dependent oxidation.

Some care must be taken in using the SPICE-SET model described here. The model assumes that the capacitances of the source and drain electrodes are large enough that charge quantization on these electrodes can be neglected. Furthermore, the model calculates only the average current but does not incorporate the stochastic nature of electron tunneling. This is a problem when frequencies approaching I/e are considered. Sometimes this SPICE model can also fail to converge at very low temperatures because a SET develops discontinuities in the differential conductance in the limit of low temperatures. This however is not a limitation, since raising the temperature of the simulation somewhat solves this problem without changing the device characteristics. Despite the two limitations of the model described above, there are circuits where it can be usefully applied. Two such circuits, the single-electron inverter and the single-electron ring oscillator, are described in the following section.

3. Single-Electron Transistor Circuits

An inverter is a basic logic element that converts a low input signal into a high output signal and a high input signal into a low output signal.^{16,17)} An inverter can be constructed by placing two single-electron transistors in series that share a common input gate (see Fig. 4). For the SPICE model to be valid, the output capacitance C_L must be large enough that single-electron effects on node 2 are not significant. Experimental realizations of single-electron inverters are described in refs. 15 and 18. Figure 4 shows the input-output characteristics of a single-electron inverter. Again, the SPICE-SET simulations agree perfectly with the Monte-Carlo simulations performed with SIMON. The parameters for this simulation were taken from ref. 15. For proper operation of the inverter, voltage gain is required. The output voltage must change faster than the input voltage in the transition region where the output changes from high to low. For the inverter in Fig. 4, voltage gain at 30 K is possible but there is no voltage gain at 77 K. The largest voltage gain that has been observed in a single-electron inverter is 5.2 at 200 mK¹⁹⁾ and the highest temperature for which voltage gain was observed was a gain of 1.2 at 27 K.¹⁵⁾ Simulations show that substantial voltage gain at room temperature does not seem possible.²⁰⁾

To investigate the speed of the inverter, nine inverters were placed in series with the output of each inverter connected to the input of the next inverter. When the input of the first inverter is driven from low to high, this signal propagates through the inverter chain. Figure 5 shows the result of this simulation. There is a delay of 90 ps at each inverter stage. The delay is largely determined by the output impedance of the inverters combined with the parasitic capacitance of the wire at the output of the inverters. The capacitance at the output of the inverters was chosen to be 200 aF. This is the capacitance of a wire with a length of about 1 μ m.

A ring oscillator is used to generate an oscillating signal. One can be built by connecting three inverters in a ring. This circuit has no dynamically stable solution, provided that the

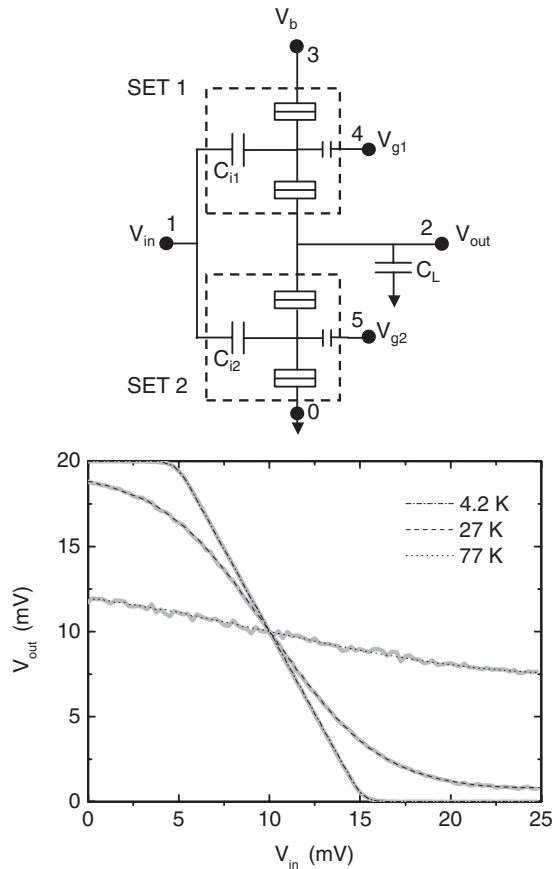


Fig. 4. A schematic diagram of a single-electron inverter and the input-output characteristics of the inverter calculated at 4.2 K, 27 K, and 77 K. The simulations performed with SPICE-SET (black lines) are compared with the ones performed with a conventional Monte-Carlo simulation program (gray lines). To generate this graph, the parameters were taken from ref. 16. All junction capacitances were set equal to $C = 1$ aF, all junction resistances were set equal to $R = 1$ G Ω , the input capacitances were $C_{in1} = C_{in2} = 2$ aF, the background charges were $Q_1 = -0.15e$, $Q_2 = 0.15e$, and the bias voltage was $V_b = 20$ mV.

speed of a single inverter stage is sufficiently faster than the signal propagation through the whole circuit. Thus, the voltage at the output of each inverter oscillates as a function of time. Figure 6 shows the ring oscillator circuit and the voltages at the outputs of the three inverters as a function of time. In the first 2 ns, the power supply is ramped up from 0 mV to 35 mV and the ring oscillator soon assumes its oscillating behavior.

4. SETs Combined with Other Circuit Elements

The circuits described and simulated above consist entirely of single-electron transistors and basically reproduce results that can be obtained using other single-electron simulation programs. The real advantage of using SPICE is that other devices such as FETs can be simulated in the same circuit with SETs. In this section circuits with SETs, FETs, and operational amplifiers are described.

One of the problems that has to be addressed in single-electronics is how the SETs will be biased. Many circuits require the SETs to be current biased. However, it is impractical to use a separate external current source for every SET on a chip. A better solution is to make current sources on chip for every SET that requires a current source. A simple

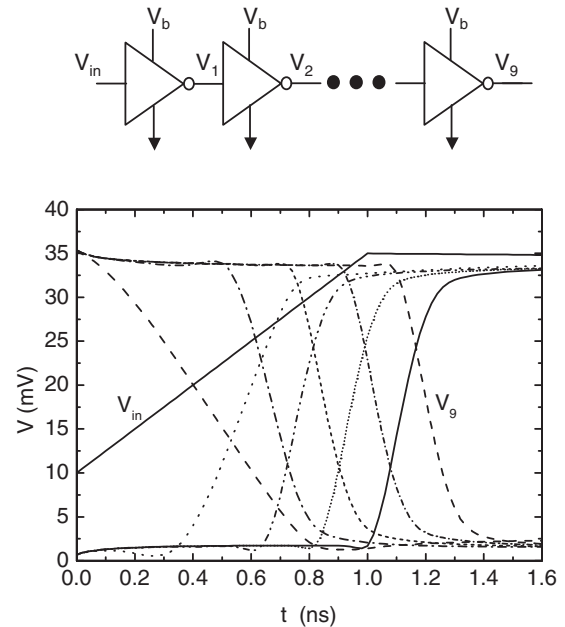


Fig. 5. The output voltages of nine inverters in series as a function of time. The inverter characteristics are the same as in Fig. 4 except that the resistances have been reduced to 100 k Ω and the bias voltage has been increased to 35 mV. The operating temperature is 4.2 K.

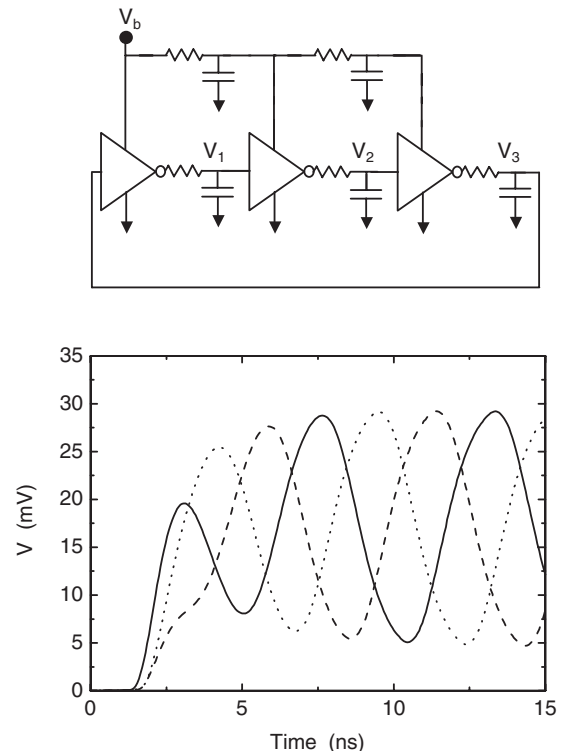


Fig. 6. The ring oscillator circuit and the voltages at the outputs of the three inverters as a function of time. Each of the triangular inverter symbols represents the circuit shown in Fig. 4. The values for the resistances and capacitances on the input of each inverter are 10 M Ω and 100 aF. The power supply is ramped from 0 mV to 35 mV in the first 2 ns. In order to get each of the inverters started at a slightly different time, resistances of the order of 1 k Ω and capacitances of the order of 0.1 pF are added to the power supply. The solid line is the voltage at the output of the first inverter, the dashed line is the voltage at the output of the second inverter, and the dotted line is the voltage at the output of the third inverter.

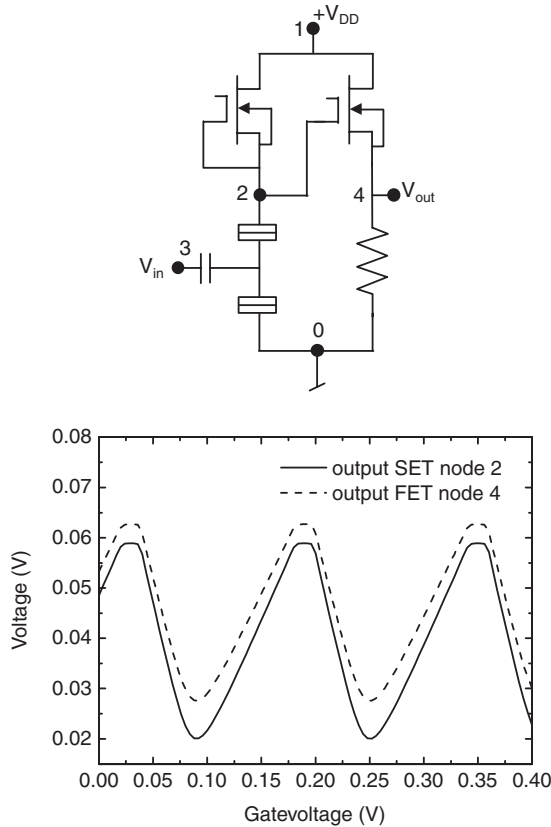


Fig. 7. The schematic of a current biased SET with a FET output stage and the corresponding SPICE simulation. The solid line is the voltage at the output voltage of the SET stage (node 2) and the dashed line is the voltage at the output of the FET stage (node 4). A voltage of 0.4 V has been subtracted from the voltage at node 4 to remove a dc offset. The parameters of the SET are the same as the ones in Fig. 3. The bias voltage is $V_{DD} = 1.5$ V, and the resistor is 10 k Ω . For the MOSFETs, a standard Shichman–Hodges transistor model was used. For the NMOS bias transistor, the transconductance was specified with the SPICE parameter $KP = 10^{-7}$ A/V² and the threshold voltage was chosen to be $V_{TO} = -1$ V, while for the NMOS source follower, the transistor parameters were $KP = 10^{-2}$ A/V² and $V_{TO} = -0.5$ V.

current source can be constructed using just one FET. Figure 7 shows a single-electron transistor that is current biased by a FET and the corresponding SPICE simulation of the circuit. A second FET is used in the circuit of Fig. 7 to buffer the output of the SET. This is one way to solve the problem of the large output impedance of SETs. It is fundamental to the operation of SETs that the output impedance must be larger than the quantum resistance (≈ 25 k Ω), otherwise the charge on the island of the SET is not well defined. For SETs that operate at high temperature, the output impedance is typically much larger. This is a problem if the output of the SET has to drive a signal a long distance across the chip. The time it takes for the output of the SET to settle to the right value is RC where R is the output impedance of the SET and C is the capacitance of the wire that carries the signal away from the SET. Thus, the high output impedance can make the response of the circuit slow. By adding the FET buffer stage at the output of the SET, the output impedance is reduced to 100 Ω , increasing the speed of the circuit greatly.²¹⁾

The thorny background charge problem can also be addressed by combining SETs with other circuit elements. This problem arises because of the tremendous charge

sensitivity of a SET. A single charged vacancy or an interstitial ion in the oxide near a SET can be enough to switch the transistor from conducting to nonconducting. The consequence of this is that when many SETs are fabricated on a chip, some of them will be conducting with zero voltage applied to the gate and some will be nonconducting with zero voltage applied to the gate. During the course of time, the charged defects often move or shift between different positions. These movements are detected by the single-electron transistors. The same kinds of charged defects are present and move in field-effect transistor circuits but most field-effect transistors are not as sensitive to charge so the consequences of these background charges are not as great. The background charge problem is probably the single greatest problem preventing the widespread use of SETs in integrated circuits.

There is a class of circuits called charge-locked loops that can automatically tune the background charge away. Figure 8 shows an example charge-locked loop circuit where a SET is current biased and feedback is used to keep the voltage across the SET constant. If charge is added at the input gate (node 3), the feedback circuit subtracts the same amount of charge from the feedback gate (node 4). The voltage change at the output is proportional to the voltage change at the input with a voltage gain set by the ratio of the input capacitance to the feedback capacitance, C_{in}/C_{fb} . In the simulation of Fig. 8,

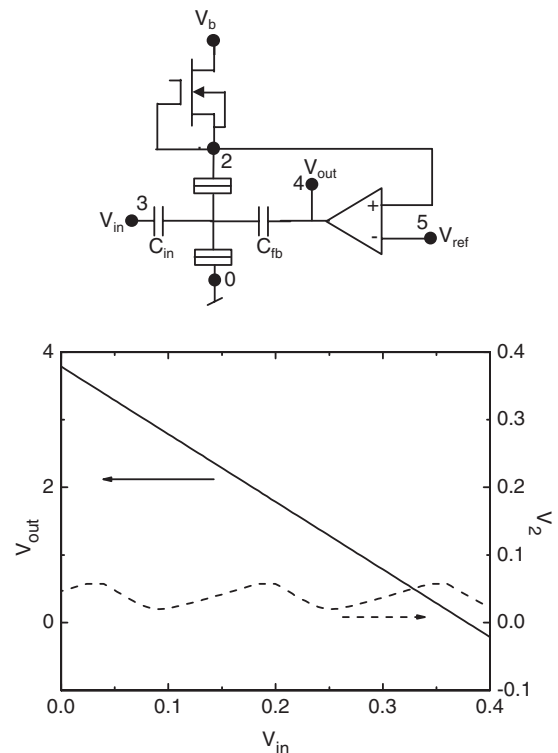


Fig. 8. The schematic of a charge-locked loop circuit and the corresponding SPICE simulation. The solid line shows that the voltage at the output is $V_{out} = -C_{in}V_{in}/C_{fb}$. In the simulation $C_{in} = 1$ aF and $C_{fb} = 0.1$ aF. The operational amplifier is a Texas Instruments TLC2201 which is powered by two voltage sources of -5 V and $+5$ V, the bias voltage is $V_b = 2$ V, and all the other parameters are the same as the corresponding ones in Fig. 7. The dashed line is the voltage at the output of the SET (node 2) when the loop is opened, i.e. when the output of the operational amplifier is disconnected from the gate capacitor C_{fb} . The voltage gain, linearity, and dynamic range are all improved by using a charge-locked loop.

the voltage gain was set to be 10. Using a charge-locked loop improves both the linearity and the dynamic range of the charge measurement. Moreover, a charge-locked loop eliminates some of the problems associated with the background charge. The output voltage always changes by $\Delta V_{\text{out}} = -\Delta q_{\text{in}}/C_{\text{fb}}$ irrespective of the background charge. This is not the only charge-locked loop circuit possible. Another way to build a charge-locked loop is to voltage bias a SET and use a feedback loop to keep the current through the SET constant. Sometimes an ac modulation of the gate charge is used to improve the charge sensitivity of a charge-locked loop.

5. Conclusions

A SPICE model for a single-electron transistor was described that implements the full orthodox theory of single-electron tunneling. This model can be combined with the standard SPICE libraries to simulate circuits of SETs and conventional semiconductor devices. The complete source code for these simulations is available on the Internet. The most promising applications for SETs involve charge sensing in metrology or the readout of few electron memories. In these applications, SETs should be integrated with field-effect transistors. The SETs provide charge sensitivity and the field-effect transistors provide voltage gain, buffer the high output impedance of the SETs, and tune the background charges.

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