Selective Solid-Phase Epitaxy of Ultra-Shallow p^+ Aluminum-Doped Silicon Junctions for Integration in Nanodevices

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To meet the demands of the next generation of CMOS, the limits of silicon integration are being pushed towards nanoscale dimensions. Exploratory research has in the past couple of years been directed towards semiconductor nanostructure growth and several successful studies have been reported [1,2]. However, the existing fabrication techniques are still far from being viable integration processes. In this paper, we present a well-controlled sub-500°C solid-phase epitaxy (SPE) process for selectively filling nanoscale contact windows with aluminum p^+-doped Si, directly applicable for integration in Si nanodevices.

The basic process flow is presented in Fig. 1. Contact windows are first opened through a thermal oxide to the mono-crystalline <100> Si substrate. Silicon-nitride spacers are used as a hard mask to anisotropically open contact windows to Si substrate. After the removal of the SiN spacers, contact windows down to 100 nm dimensions were obtained in a reproducible way (Fig. 2a). Physical vapor deposition (PVD) of a thin layer of aluminum and amorphous silicon (α-Si) is then performed in the same vacuum system. The epitaxial growth was induced by annealing at temperatures between 350 and 500°C, which is far below the 577°C eutectic point of the Al/Si alloy. Initiated first in the corners of the contact windows, presumably due to a stress driven process, the crystal growth, fed from the α-Si layer via a fast diffusion process in the Al layer [3], occurs preferably on the exposed silicon substrate rather than on the surrounding oxide and stops abruptly when the crystal protrudes above the Al layer. Lateral growth proceeds until the contact window is entirely filled. For contact windows smaller than 500 nm wide, a single crystal will fill the entire contact window. The epitaxial growth has been verified (Fig. 2b) by high-resolution transmission electron microscope (HRTEM). The grown material is highly p^+-doped with aluminum. The abruptness of the doping transition has been verified by capacitance-voltage doping profiling from the substrate to the SPE crystal and these measurements confirm that no Al diffuses into the bulk-Si substrate even at 500°C. The doping level of the SPE p^+ Si region is found to be above the known solid solubility of Al in Si about $1 - 3 \times 10^{18}$ cm^{-3} [4]. The height of SPE Si is determined by the initial thickness of the metal layer, and is therefore well controlled even at nanoscale dimensions.

The quality of the SPE Si has been extensively investigated by fabricating and characterizing electrical devices such as ultra-shallow p^+n diodes, p^+ contacts, and p^+ emitters in simple p^+np bipolar junction transistors (BJTs). The contacts could also be directly integrated as source/drain contacts in p-type CMOS transistors. Despite the low-processing temperature, near-ideal diode and BJT characteristics were obtained, indicating an exceptionally low defect density at the SPE to bulk Si interface. The ideality of the p^+n diodes (with an ideality factor of 1.02) is remarkable since the doping transition is situated at the growth interface, which hence must be situated within the junction depletion region. Without SPE, an Al to n-Si Schottky diode is formed that has a two-decades-higher saturation current (Fig. 3). The contact resistance to both p^-- and p^+-bulk silicon regions was found to be low ohmic and the total contact resistivity of the SPE contact plus metallization was measured to be at most 10^{-7} ohm-cm^2 (Fig. 4). The measurements clearly show that the contact resistivity increases slightly when the SPE temperature decreases, presumably due to lower Al doping level. A 50 nm-thick SPE-Si region was used as an emitter in a p^+np BJT (Fig. 5). An analysis of the transistor characteristics indicates near-ideal forward base and collector currents, and a current gain $h_{FE} = I_C / I_B$ of about 3 (Fig. 6).

The SPE p^+-doped Si demonstrated in this work has several remarkable properties, particularly in view of the low processing temperatures. The epitaxial growth seen in the HRTEM image has been proven by electrical characterization of the p^+n diodes to be defect free over the wafer and from wafer to wafer. The transition to the p^+ doping of the SPE island is abrupt and the height of the island has been shown to be well-controlled down to 25 nm. The high quality of the SPE Si and the diodes that can be fabricated with it make this a versatile CMOS compatible module for the location- and dimension-controllable integration of Si nanodevices.

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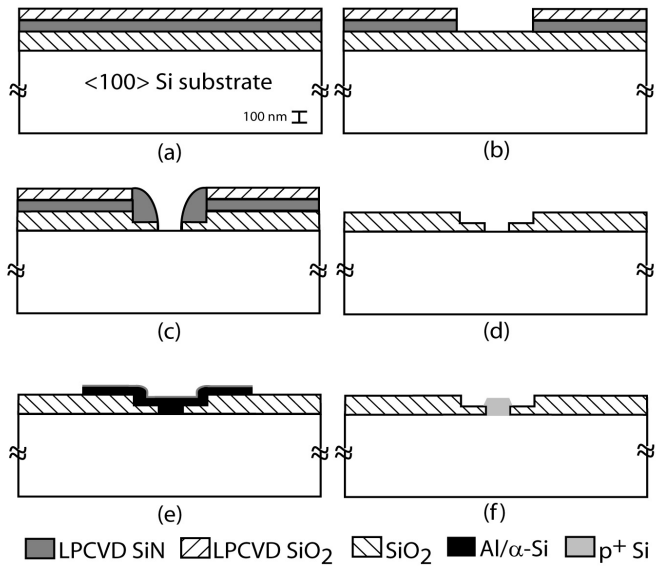

Fig.1: The solid-phase epitaxy sequence. (b) Contact window definition. (c) SiN spacer formation. (d) Spacer removal (e) PVD deposition of Al/α-Si and anneal with transport of α-Si through Al to the c-Si surface. (f) Epitaxial Si (after Al removal).

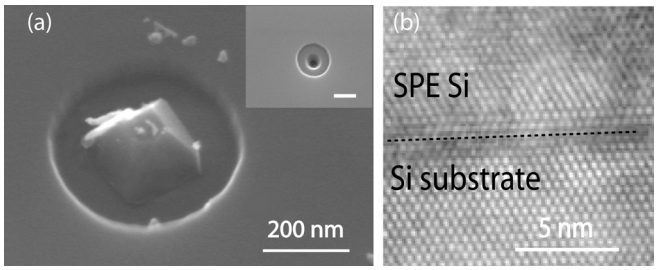

Fig. 2: (a) SEM micrograph of the contact window after silicon SPE (and Al removal). A crystal grows at the interface with the Si substrate. Overgrowth on the oxide is clearly observed. The inset represents the contact opening before the SPE growth. The scale bar is 200 nm. (b) HRTEM image of the growth interface.

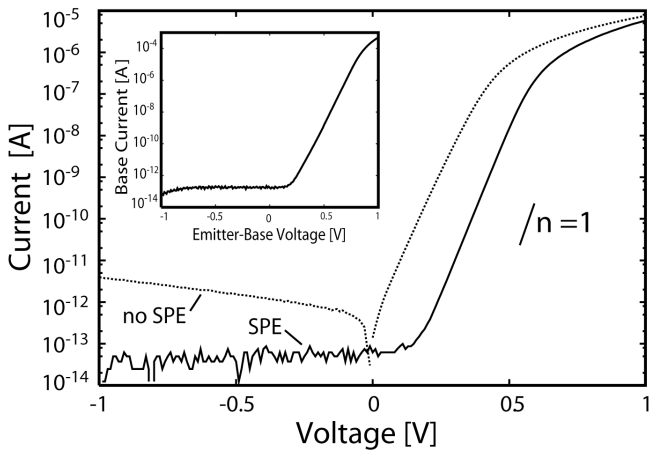

Fig. 3: The current-voltage characteristics of $1\times1\,\mu m^2$ junctions fabricated on a $2-5\ \Omega$·cm n-type substrate. The solid line is for a SPE p^+n diode with 100 nm thick p^+ Si. The inset represents the base current of a p^+np where the emitter is formed by a 25 nm-thick SPE p^+ Si region grown at 400°C.

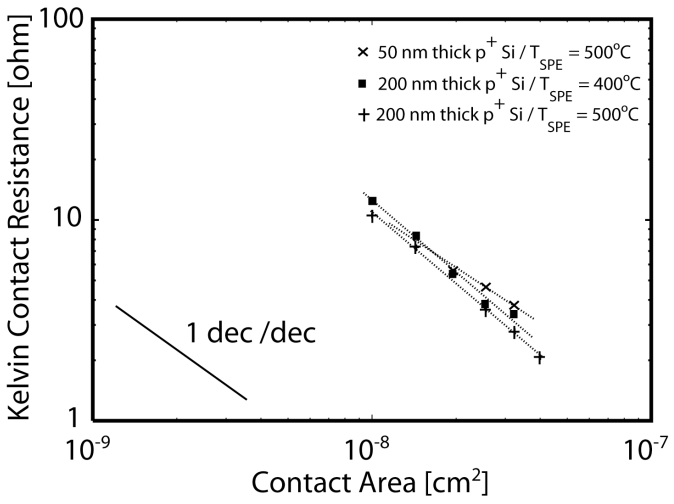

Fig. 4: Contact resistance of SPE p^+ filled contacts measured on special Kelvin test structures with low-ohmic p^+ diffusion taps.

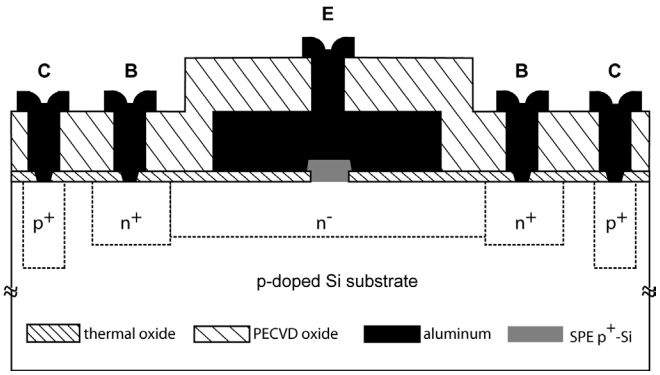

Fig. 5: A schematic cross section of the p^+np bipolar junction transistor in which the emitter is deposited by SPE. The base doping is $2\times10^{17}\,cm^{-3}$.

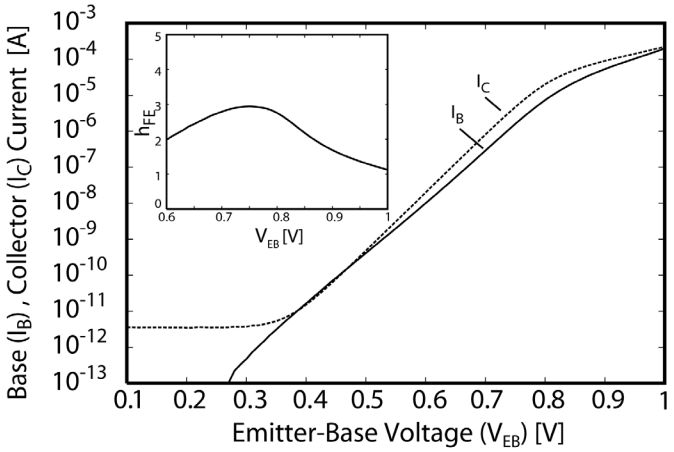

Fig. 6: Measured Gummel plot of a p^+np BJT with a 50 nm-thick and $0.7\times0.7\,\mu m^2$ wide SPE p^+ Si emitter. The SPE growth occurs at 400°C. The inset shows the corresponding current gain (h_{FE}) function of the emitter/base voltage.