Fabrication and numerical analysis of nanoscale silicon pillars for IC applications

Y. Civale, P. Hadley, L. K. Nanver, E. J. G. Goudena and J. Slabbekoorn

***Abstract*— A technique based on standard lithography tools is presented for the fabrication of silicon pillars. A post-processing oxidation is performed to consume silicon and remove all defects induced by plasma etching. By using this technique, diameters of about 100 nm are achieved. MEDICI simulations have been performed to model electrical behavior of p^+ silicon pillars embedded in a dielectric shield on top of a n-doped Si substrate. The simulation results show the importance of the surrounding dielectric and the doping profile on the device properties.**

***Index Terms*—nanoscale devices, silicon nanowire, bottom-up approach, p/n junctions.**

I. Introduction

The growth of semiconducting nanowires has provided new routes to the manufacture of complex nanoscale three-dimensional semiconducting structures. One of the appealing aspects of nanostructures is that it is possible to epitaxially grow materials with large lattice mismatches on top of each other since significant strain does not accumulate in a small structure. Several nanowire growth methods have been developed, such as template-assisted synthesis, laser ablation [1], chemical vapor deposition (CVD) [2], electrochemical deposition [3], or the vapor-liquid-solid (VLS) approach [4-6]. By using these different techniques, a large variety of semiconducting nanowires have been reported. Indium phosphate [7], gallium nitride [8], germanium [9] and silicon [10] nanowires have been fabricated over the past few years. Prototype transistors, light-emitting diodes, lasers, charge sensors, chemical sensors, and mechanical sensors, all using semiconducting nanowires as a building block, have been also reported [11].

However, not all of these nanowires can be incorporated in a straightforward way into a full CMOS compatible process. Indeed, most of these techniques use materials, such as gold or iron, that are not compatible with front-end Si processing because they diffuse and deteriorate the device performance. In addition, the ability to control the dimensions and the position of the nanowires, which is an essential requirement for future IC applications, is not provided by a purely bottom-up growth mechanism.

From this point of view, the top-bottom approach is an interesting alternative because it has the advantage of reliability and reproducibility. By using the techniques developed for semiconductor industry, the method appears to be more controllable for future device applications. In this study, a technique based on standard lithography tools is presented for the fabrication of silicon pillars. A post-processing oxidation is performed to consume silicon and remove defects induced by the plasma etching. By using this technique, the diameter is reduced to about 100 nm. To support the experimental work and investigate the effects of scale reduction on the electrical properties of nanodevices, numerical simulations were performed using MEDICI on contacted cylindrical Si pillar-like p/n junctions.

II. Fabrication

The process flow for the fabrication of silicon nanopillars is presented in Fig. 1. A four step-process was used to fabricate 500 nm-tall silicon pillars on a <100> Si substrate. The substrate was first oxidized at 1100ºC to grow 400 nm thermal silicon oxide. Then, this layer was etched by reactive ion etching (RIE) in order to form an approximately 500 nm wide silicon oxide mask. Additional wet etching for 30 s, keeping the photoresist on top, was performed in order to reduce the size of the oxide mask. Then plasma Si etching was performed using HBr / Cl_2. The as-obtained pillars are about 250 nm wide and 0.5 μm tall (Fig. 2.). To obtain such small structures by using conventional lithography equipment, a study has been done on the experimental parameters in order to find the optimal photoresist thickness / exposure energy combination that yields stable and reproducible process conditions.

The pillars are slightly larger at the base of the structure. This is a well-known effect induced by plasma etching. In the fabrication process we developed, this can also be introduced by the shape of the oxide mask itself. Indeed, due to the inhomogenous additional wet etching step done before the Si plasma removal, the tapered shape of oxide masks is directly reproduced the silicon during the plasma etching. The sample was then oxidized to remove defects induced by plasma etching and to thin down the Si core [12].

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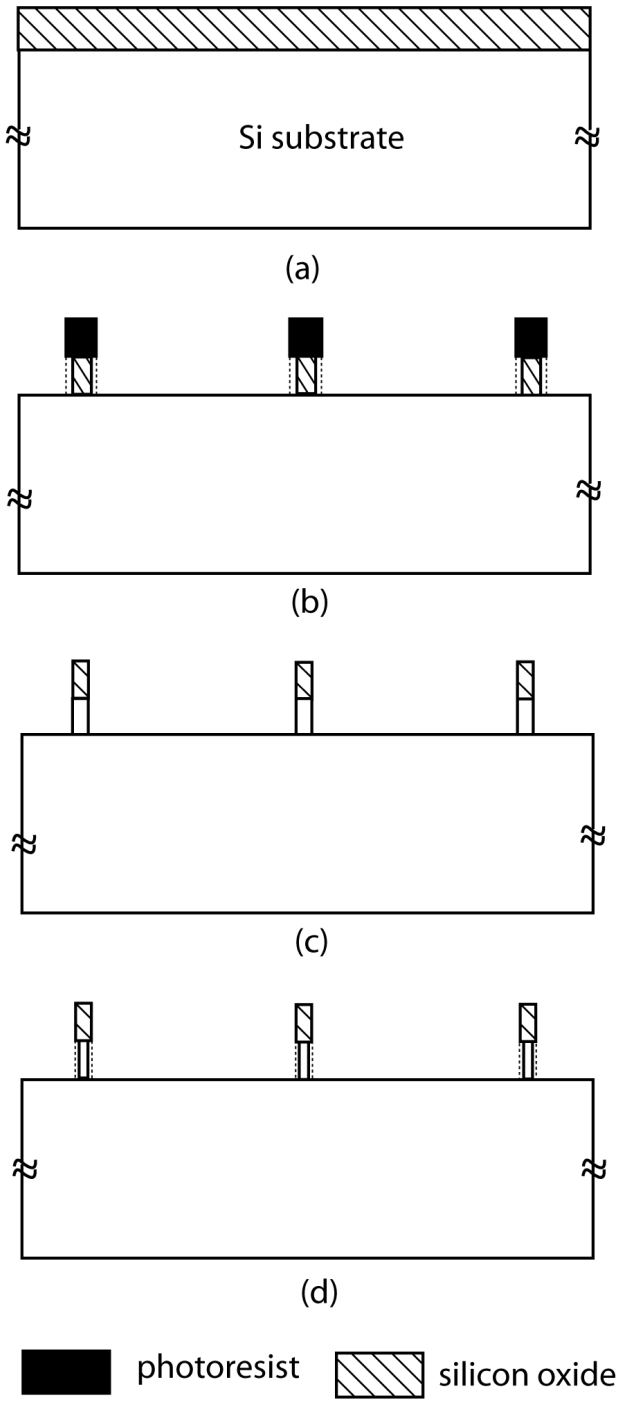

Fig. 1. Process flow for fabrication of silicon pillars. (a) Deposition of 400 nm thermal oxide. (b) Oxide plasma etching. Additional wet etching is performed to decrease the width of the oxide mask. (c) Silicon plasma etching. (d) Oxidation cycle to reduce the dimensions of as-obtained silicon pillars.

In order to reduce the stress in the base of the pillar, a 30 nm-thick oxidation cycle was performed at 850ºC. The oxide grown on the sidewalls was then etched away by soft chemical etching in hydrofluoric acid HF 1:7. Repeating the cycle of oxidation / oxide removal two times resulted in thinner silicon structures with a diameter of about 100 nm.

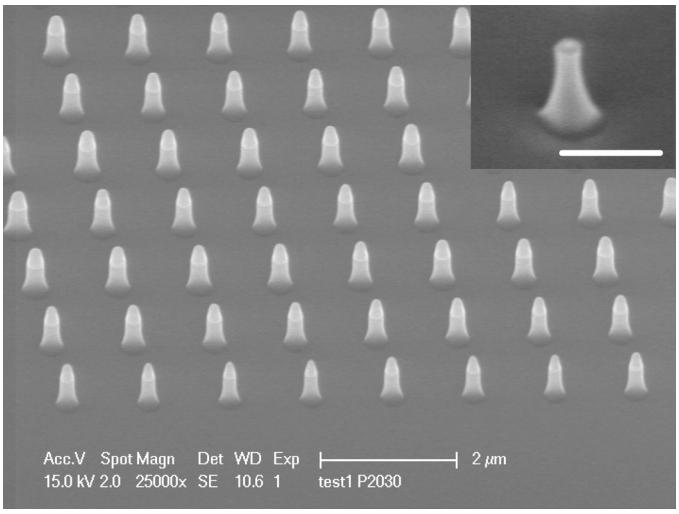

Fig. 2. SEM micrograph of silicon pillars obtained by plasma etching. The oxide mask is still on the pillars. The pillars are 0.5 long and approximately 250 nm wide. The rounding shape is due to additional wet etching and the silicon plasma etching. The inset shows the pillar after a 30 nm thick thermal oxidation and soft chemical etching in HF 1:7. The diameter of pillar after one oxidation cycles can be reduced down to approximately 100 nm. The scale bar is 250 nm.

III. Simulation

A. Device structure

Using MEDICI [13], we simulated the behavior of a Si pillar-like p/n junction embedded in dielectric material. The simulated device is shown on Fig. 3. The objective was to study the effect of downscaling and surrounding materials on contacted p/n junctions. The simulated structure was a 500 nm-tall cylindrical p^+ silicon pillar embedded in a dielectric shield, on top of n-doped Si substrate. The doping of the n-doped substrate was 10^{15} cm^{-3} and 10^{17} cm^{-3} for n^- and n^+ respectively. Simulations were performed using silicon oxide, silicon nitride or sapphire as dielectric materials. Different Si pillar diameters, 100 nm, 50 nm, and 20 nm were investigated. The flexibility of the nanoscale Si pillar process makes it interesting to study also the influence of the vertical position of the p/n junction in the pillar. In that case, two different configurations have been simulated in which the junction between the p^+ and n^+-doped regions is at the substrate interface between the substrate and the Si pillar or inside the pillar itself.

B. Simulation results

The simulation results show first the influence of the scale shrinking on device properties. Due to the continuity of electric displacement, the electric field is lower at the lateral interface between the Si core and the dielectric and consequently the depletion region is wider (Fig. 4.). The electric displacement is defined by $D \approx \varepsilon_r \cdot \varepsilon_o \cdot E$, in which D, ε_r, ε_o, and E are respectively the electric displacement, the permittivity of the material, the permittivity

of free space and the electric field. This phenomenon is negligible for large-scale p/n junctions but when the dimensions of the devices are reduced it becomes predominant. An interesting consequence of the diameter reduction is the higher breakdown voltage compared to a bulk device with the same doping profile.

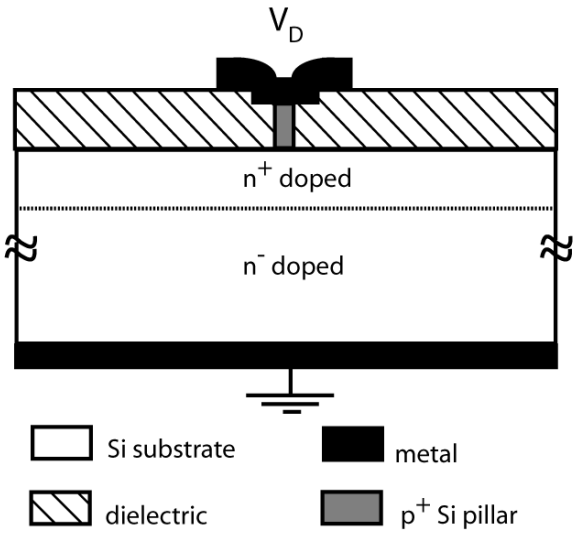

Fig. 3. The cross section of the simulated structure. In this configuration, the junction between the p^+ and n^+ regions is situated at the substrate / pillar interface.

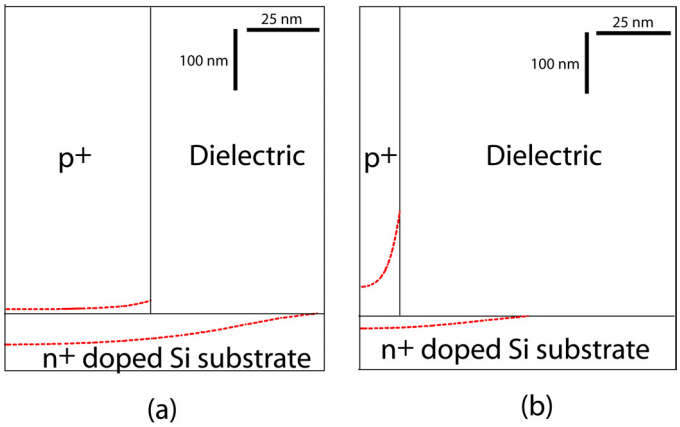

Fig. 4. Edges of the depletion region in reverse bias (V_D = -0.5V). (a) 100 nm wide p^+ Si pillar (b) 20 nm wide p^+ Si pillar. In both case, the dielectric material is silicon oxide. The doping of the p^+ and n^+ regions is 10^{18} cm^{-3} and $10^{17}cm^{-3}$, respectively.

This phenomenon has been verified for different dielectric materials. Structures using silicon oxide, silicon nitride, and sapphire, where the permittivity ε_r is 3.9, 7.5 and 12 respectively, have been simulated. The results are presented on Fig. 5. When the dimensions of the device become small, the depletion region width is also determined by the position of the p/n junction in the structure we simulated. Indeed, as we have seen in Fig. 4, the effects of surrounding dielectric material become, in that case, predominant.

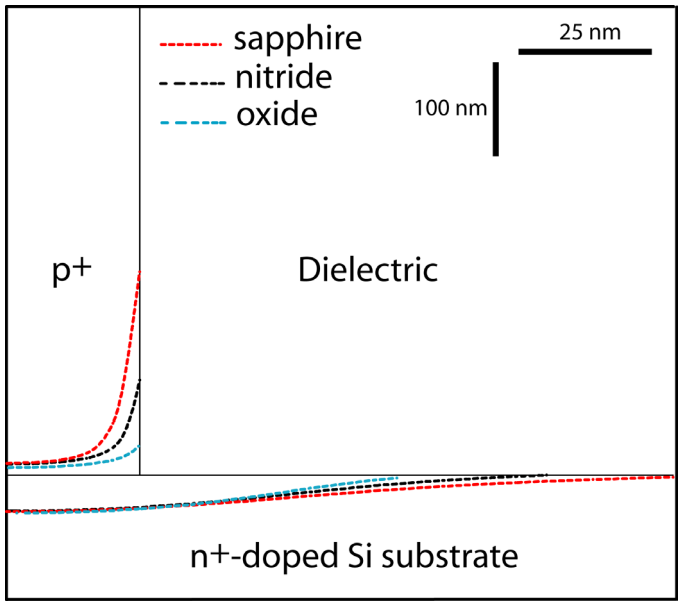

Fig. 5. Edges of the depletion region function of nature of dielectric material in reverse bias (V_D = -0.5V). In all case, the diameter of the conducting pillar is 50 nm, the doping of the p^+ and n^+ regions is 10^{18} cm^{-3} and $10^{17}cm^{-3}$, respectively.

Consequently, a nanoscale p/n junction inside the Si pillar has a much wider depletion region and consequently a higher breakdown voltage compared to a structure in which the junction is at the interface between the small structure and the Si substrate as shown in Fig. 6.

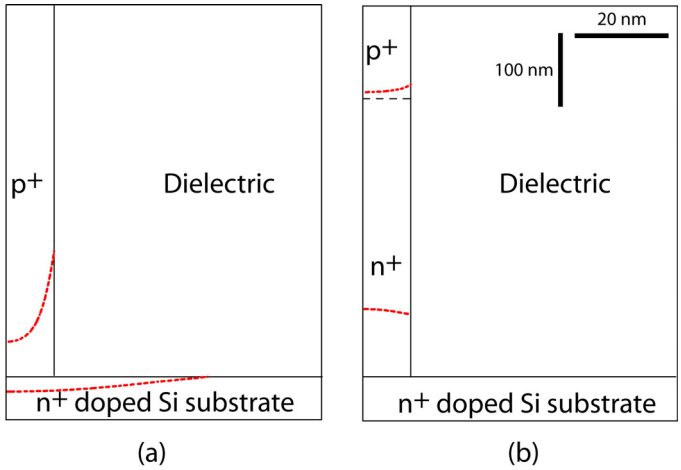

Fig. 6. Edges of depletion region function of position of the p/n junction. (a) The junction is situated at the interface between the pillar and the substrate. (b) The junction is situated inside the wire. In both cases, the doping of the p^+ and n^+ region is 10^{18} cm^{-3} and 10^{17} cm^{-3} respectively. The diameter of Si pillar is 20 nm and the dielectric material is silicon oxide.

IV. Conclusion

In this paper, we presented a simple and controllable method to obtain nanoscale Si pillars by plasma etching. Using well-known techniques, this method is fully compatible with standard IC processes. Pillars with a diameter of about 100 nm have been obtained after plasma silicon etching and oxidation

cycle. MEDICI simulations of contacted Si p/n junctions were performed. The results of the simulations give a better understanding of the predominant effects of downscaling on device properties, particularly the importance of edge effects and the surrounding material. A higher breakdown voltage is predicted for nanoscale p/n junctions.

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