

A new process for nanometer scale devices

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ABSTRACT

A new process employing e-beam lithography and a self-aligned two angle shadow evaporation has been developed to fabricate 10 nm tunnel junctions and split leads with gaps of 2-5 nm. The fabricated Al/Al_xO/Al tunnel junctions on a SiO₂/Si substrate had a capacitance of 20 aF. These tunnel junctions were incorporated in single electron tunneling circuits where the small capacitance is essential. Single electron tunneling transistors with threshold voltages of 3 mV were fabricated using this process. The object of closely spaced leads (2-5 nm) was to contact individual molecules for electrical characterisations. Further improvements of this process for a triple angle shadow evaporation will be discussed.

Keywords: Coulomb blockade, single electron tunneling, threshold voltage, charging energy, electron beam lithography, self-aligned shadow evaporation, metallic junction, SET transistor, junction capacitance, parasitic capacitance

1 Introduction

The Coulomb blockade of electron tunneling occurs in systems of two tunnel junctions in series if the voltage bias is below the threshold voltage $V_{th} = e/C_{\Sigma}$.^{1,2} Here C_{Σ} is the total island capacitance $C_{\Sigma} = C_1 + C_2 + C_g + C_o$ where C_1 and C_2 are the capacitances of the two junctions respectively, C_g is the gate capacitance, and C_o is the stray capacitance to the ground which is usually negligible compared to the other capacitances.³ For bias voltages above the threshold voltage, electron tunneling through the junctions occurs and the current that flows is a periodic function of the gate voltage with a periodicity of the elementary charge of an electron, e . A variety of applications for SET transistors have been proposed,³⁻¹⁵ however presently all these applications can only be realized at very low temperatures ($\leq 1K$). This is because the Coulomb blockade is suppressed for temperatures where $k_B T \geq e^2/2C_{\Sigma}$. To achieve high temperature applications, it is now urgently required to develop nano-fabrication techniques for increasing the charging energy E_c by reducing the island capacitance C_{Σ} , especially the tunnel junction capacitances C_1 and C_2 . A low gate capacitance C_g in C_{Σ} is easy to be achieved.

The progress in fabricating ultra small metallic junctions with the conventional nano-fabrication technique, i.e. high resolution electron beam lithography (EBL) combined with two angle shadow evaporation¹⁶ has reached the

limit determined by the thickness of the metallic film, which is about 20~30 nm. Further reducing the junction size by developing new fabrication processes has attracted increasing interests. Götz presented a SAIL process different from the conventional technique.¹⁷ The technique includes in total six process steps and is therefore rather complex. The resulting junction area is about $70 \times 70 \text{ nm}^2$ with a maximum operation temperature of 1 K. Recently a very profound progress toward to higher temperature operation of SET transistors has been achieved by Nakamura, et al.¹⁸ By a triple shadow evaporation, they successfully reduced the junction size down to ~10 nm and meanwhile eliminated the parasitic capacitance between the island and the leads such that the charging energy has been increased up to 11 meV corresponding to an operation temperature of 100K. However, the problem arising from the triple evaporation is the large layout size and many unwanted leads of each SET transistor, which may cause difficulties in practical applications in integrated circuits in the future.

In this paper, we demonstrate a novel technique for the fabrication of ~10 nm metallic junctions in SET transistors by a self-aligned shadow evaporation (SASE) process after high resolution electron beam lithography. With this technique, we also successfully fabricated closely spaced leads with a gap as narrow as 2 ~ 5 nm, which can be used for the electrical characterisation of single molecules. This progress leads to a proposal for further developing this technique for smaller junction capacitance which will be discussed in this paper.

2 The SASE Process and Results

The fundamental principle of the self-aligned shadow evaporation (SASE) process is outlined as follows: With a specially designed pattern for the SET transistors as shown in Fig. 1. First the layer that will form the metal island is deposited at an angle of 14° . This deposition angle gives the island a sharp edge. A thin lead electrode layer is then deposited over the edge of the island and the lead interrupted by the island edge. The junction is formed where the lead touched the edge of the island. Thus, the junction area is actually defined by the lead width times the lead thickness. Here, the *shadow* is provided by the edge of the island in contrast to a hanging bridge which is used in conventional shadow evaporation. With our high resolution electron beam pattern generator (*Leica* EBPG HR-5) it is possible to write a line with a width narrower than 10 nm. A lead thickness as thin as 5 nm can be well controlled by a quartz-crystal thickness monitor during evaporation. Compared to the conventional two angle shadow evaporation, our SASE process does not need any extra steps and should be used as conveniently as the conventional technique.

In details the SASE process has the following steps: a double layer of e-beam resists, PMMA/MAA (350 nm) and 950K PMMA (50 nm), was spun on Si substrates with a $0.2 \mu\text{m}$ thermally oxidised SiO_2 top layer. The designed pattern (see Fig. 1) was written with a high energy (100 keV) electron beam with a focused spot size of 2~5 nm. The most critical step in SASE process is the modified two angle shadow evaporation in an high vacuum chamber. As indicated in Fig. 1, the first Al evaporation for the island base electrode (30 nm) was done at an incident angle of 14° , resulting in a vertical edge on one side of the island. This vertically sharp edge on the island electrode was used as a shadow for the second layer of Al and its steep profile was essential for breaking the overlapping part off the leads. The tunnel barrier Al_2O_3 was then formed by oxidising this Al layer in 10^{-2} τ oxygen pressure for 2 minutes. Figure 2 is the SEM photo picture taken at a tilted angle of a fabricated SET transistor, which demonstrates the vertical edges on the right side of the island. The second Al layer (10 nm thick) evaporation deposited perpendicular to the substrate. The difference of the two evaporation angles leads to a shift of the two transferred patterns on the substrate such that the two thin leads (about 10 nm in width) were deposited across the sharp edges of the island electrode. Thus, the overlap part on the island area was disconnected by the sharp edge. Consequently, the small junction was self-aligned at the bottom of the sharp edge. The junction area is determined by the cross-sectional area of each thin lead, $10 \times 10 \text{ nm}^2$. Figure 3 is a SEM photo of a fabricated SET transistor with two metallic junctions of $10 \times 10 \text{ nm}^2$ by this SASE process. The tunnel resistance for each of the junction was about 5 M Ω .

For low temperature characterisation of the metallic junctions, we fabricated some SET transistors by SASE

process where the width of both the lead and the island was 200 nm. The characterisation was performed in a ^3He cryostat in a 2 T magnetic field to keep the junctions in the normal state. Figure 4 shows the current-voltage characteristics at 0.5 K. A threshold voltage of 3 mV was measured, corresponding to the capacitance of 20-25 aF for each junction. From the oscillation periodicity in the current vs gate voltage (not presented) the gate capacitance was measured to be 7 aF.

Although the junction capacitance has been greatly reduced by our SASE process, compared to the conventional process, it is still much higher than that reported by a triple evaporation process¹⁸ for the same size ($10 \times 10 \text{ nm}^2$). The reason will be discussed in the next section.

In our SASE process described above, we emphasized that the incident angle θ_2 for the second Al layer evaporation must be strictly set to be vertical for aligning the two tips of the two thin leads to the sharp edges for making ultra small metallic junctions. But, if we deliberately set the second incident angle to be $\theta_2 = -4^\circ$ or -6° , the two deposited thin leads can be disconnected from the base electrodes with a very small gap due to the larger shadow created by the base electrode. In this way, closely spaced leads can be fabricated, which are shown in Fig. 5. Gaps of 2~5 nm between the leads were measured from the picture taken by our high resolution Hitachi 900 SEM. This nanometer gap is of the same order as the length of some polymer molecules. After this SASE process, some polymer films can be immediately deposited on to the samples before lift-off. Some individual molecules should be located in between the spaced leads. Therefore, this process can also be applied to studying the electrical characterisation of individual molecules.

3 Discussions

3.1 The parasitic capacitance between the island and the leads

As mentioned in the previous section, for the same junction area ($10 \times 10 \text{ nm}^2$) our junction capacitance is around 20~25 aF, whereas the capacitance reported from Nakamura¹⁸ et al., is about 3 aF. Different oxidation conditions for the tunnel barrier can vary the tunnel resistance exponentially but not the capacitance. The parasitic capacitance between the leads and the island should be responsible for the unwanted contribution to our junction capacitance. In our measured SET transistors the distance between the lead and the island is about 50 nm and the width of both the island and the lead is about 200 nm, giving rise to a significant parasitic capacitance in parallel to the real junction capacitance. The measured junction capacitance is actually the sum of these two capacitances. We have calibrated this parasitic capacitance by using a SET transistor with gate that was fabricated in a similar manner as the SASE junctions. From the periodicity of the Coulomb blockade oscillations this lead-to-island capacitance was measured to be $100 \text{ aF}/\mu\text{m}$. So we can approximately estimate the parasitic capacitance between the island and the lead in the measured SET transistor to be 20 aF. If we subtract this parasitic capacitance from the measured junction capacitance (25 aF), we find the real junction capacitance in the same order as Nakamura's.

3.2 The extension of SASE process

To reduce the parasitic capacitance between the lead and the island, we can make narrower islands and leads. However, if we look at the schematic structure for the SET transistor in Fig. 1, we see two extra capacitors coupling the island to the leads. During the SASE process, we usually evaporate the third layer of Al with a larger angle after the second layer evaporation for increasing the extra capacitance as large as possible. This helped to remove the effect from the extra capacitors. But, if the island and the leads are narrowed, this effect of extra capacitor is not negligible.

To overcome this disadvantage in this SASE process, we propose a new scheme as the extension of the SASE process for completely removing the extra capacitors, which is schematically shown in Fig. 6. With a self aligned triple shadow evaporation (SATSE), the central part becomes the island (~ 10 nm wide) and its two ends connect to the two sharp edges of the leads respectively, forming two tunnel junctions. In this SATSE process, the lead separation and the incident angles should be carefully designed.

4 Conclusions

We have successfully fabricated 10×10 nm² metallic tunnel junctions by a recently developed self-aligned shadow evaporation (SASE). The junction capacitance has been reduced by one order of magnitude compared to the conventional shadow evaporation method. This SASE process also enables us to fabricate closely spaced metallic leads (1-5 nm). However, when the junction area becomes small, the parasitic capacitance between an island and a lead becomes more important. For eliminating the unwanted parasitic capacitance we proposed a new process as the extension of the SASE process described in this paper.

5 REFERENCES

- [1] G.-L. Ingold and Yu. V. Nazarov, Chapter 2: "Charge Tunneling Rates in Ultrasmall Junctions" in "Single Charge Tunneling (Coulomb Blockade Phenomena in Nanostructures)" *Nato ASI Series, Series B: Physics* ed. H. Grabert and M.H. Deaver, Vol. 294, pp.21-107 Plenum Press, New York and London, 1992.
- [2] T.A. Fulton and G.D. Dolan, *Phys. Rev. Lett.* Vol.59, pp.109-(1987).
- [3] S.M. Verbrugh, "Development of a single electron turnstile as a current standard", Ph.D. Thesis, Faculty of Applied Physics, Delft University of Technology, Delft, the Netherlands, 1995.
- [4] D.V. Averin and K.K. Likharev, Chapter 9: "Possible Applications of the Single Charge Tunneling" in "Single Charge Tunneling (Coulomb Blockade Phenomena in Nanostructures)" *Nato ASI Series, Series B: Physics* ed. H. Grabert and M.H. Deaver, Vol. 294, pp.311-332, Plenum Press, New York and London, 1992.
- [5] P. Delsing, et al, *Phys. Rev. Lett.* Vol. 63, p.1861(1989).
- [6] L.J. Geerligs, et al, *Phys. Rev. Lett.*, Vol.64, p.2691(1990).
- [7] H. Pothier, et al, *Physica B* 169, p. 1598(1991).
- [8] J. Martinis, et al, Report at LT-20 (Eugene, OR, August 1993).
- [9] A.N. Korotkov, et al, "Single Electron Tunneling and Mesoscopic Devices", ed. H. Koch and H. Lübbig, p.45 Springer, Berlin, 1992.
- [10] D.V. Averin and K.K. Likharev, *J. Low. Temp. Phys.* Vol.59, p347(1986).
- [11] K.K. Likharev, *IEEE Trans. on Magn.* 23, p.1142(1987).
- [12] K.K. Likharev, et al, *IEEE Trans. Magn.* Vol.25, p.1436(1989).
- [13] J.R. Tucker, "Complementary digital logic gates on the "Coulomb blockade"", *J. Appl. Phys.* Vol. 72, No. 9 pp.4399-4413 (1992).
- [14] A.N. Korotkov, R.H. Chen, and K.K. Likharev, *J. Appl. Phys.* Vol.78, p.2520(1995).
- [15] E.H. Visscher, "Technology and applications of single-electron tunneling devices", Ph.D. Thesis, Faculty of Applied Physics, Delft University of Technology, The Netherlands, 1996.

- [16] G.J. Dolan, Appl. Phys. Lett. Vol.31, p.337 (1977).
- [17] M. Götz, K. Blüthner, W. Krech, and A. Nowack, "Self-Aligned In-Line Tunnel Junctions for Single-Charge Electronics", J. Appl. Phys. Vol.78, No.9, pp.5499-5502 (1995).
- [18] Y. Nakamura, C. Chen and J.S. Tsai, "100-K Operation of Al-Based Single-Electron Transistors", Jpn. J. Appl. Phys. part2, Vol.35, No.11A, pp. L1465-L1467 (1996).

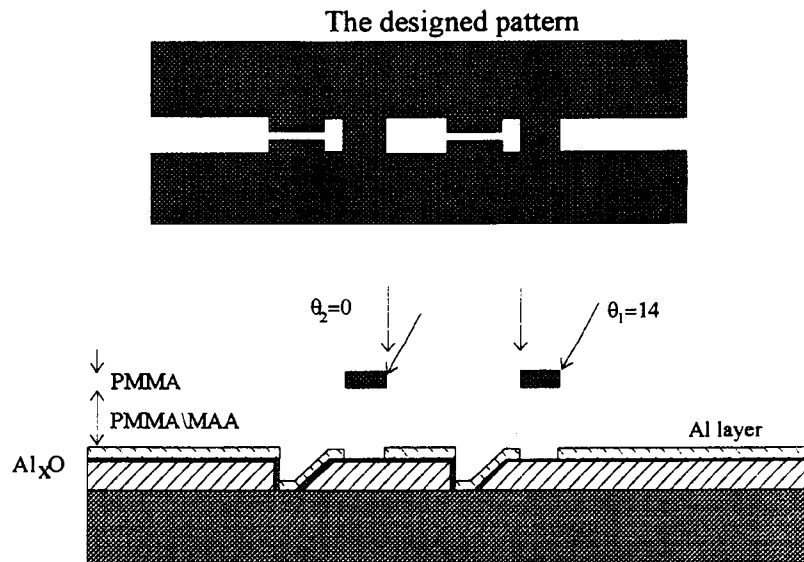


Figure 1. The schematic demonstration of a self-aligned shadow evaporation for the fabrication of ultra small metallic junctions. θ_1 and θ_2 are the incident angles for the first layer and the second layer evaporation, respectively.

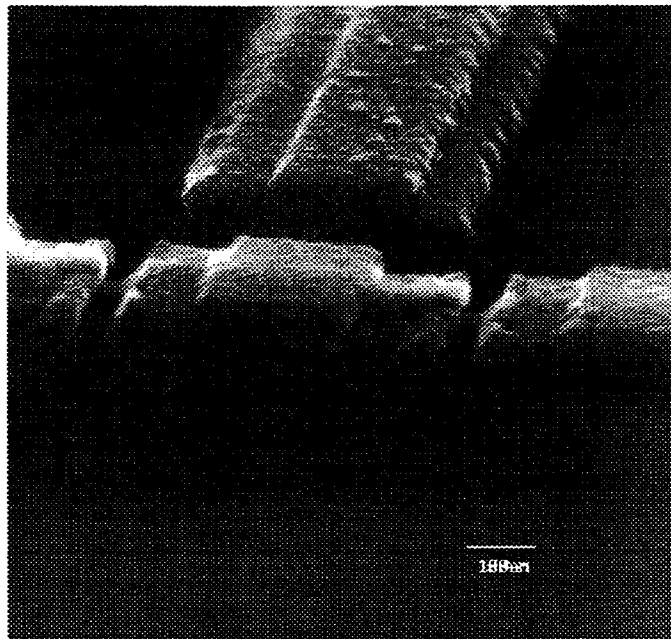


Figure 2. The SEM photo picture for the fabricated SET transistor. On the right side of the island (the central conductor) there is a vertical sharp edge such that the lead of the second layer is broken at the edge and a junction is formed on the bottom of the edge.

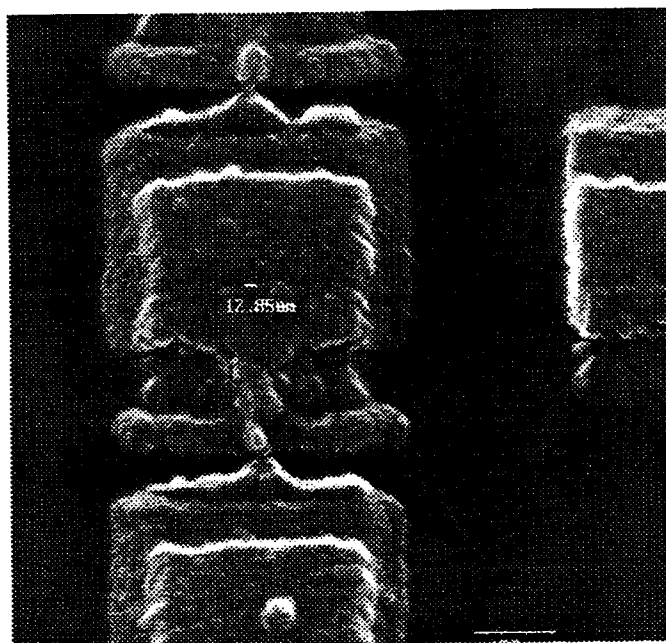


Figure 3. The SEM photo picture of a fabricated SET transistor. The 12 nm long white bar is for the length scaling, which measures our junction size to be about 10 nm at one direction.

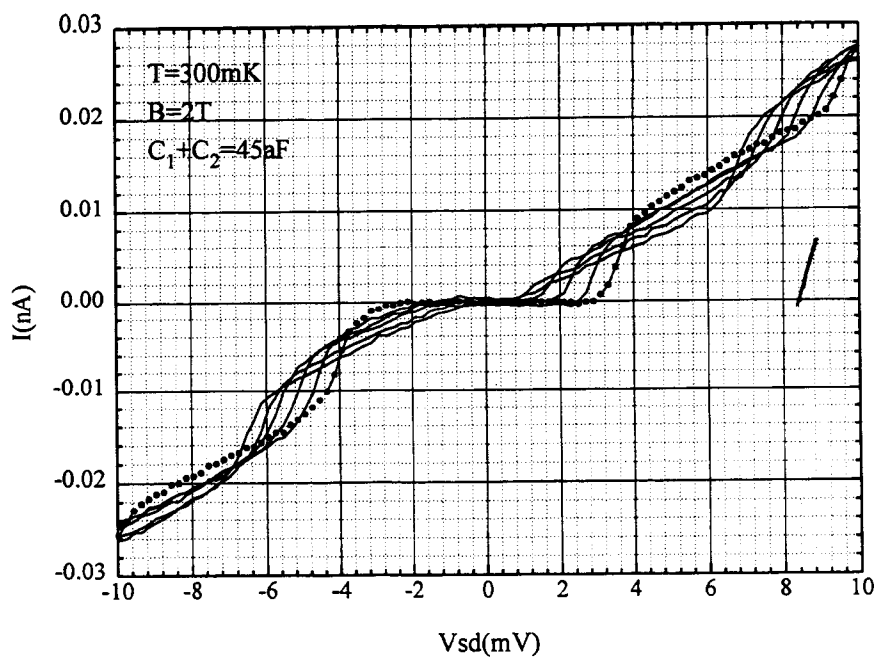


Figure 4. The measure I-V curves at various fixed gate voltage at 0.5K in 2 Tesla magnetic field. The curve with dots is measured with the offset charge of zero, which exhibits the threshold voltage of 3 mV.

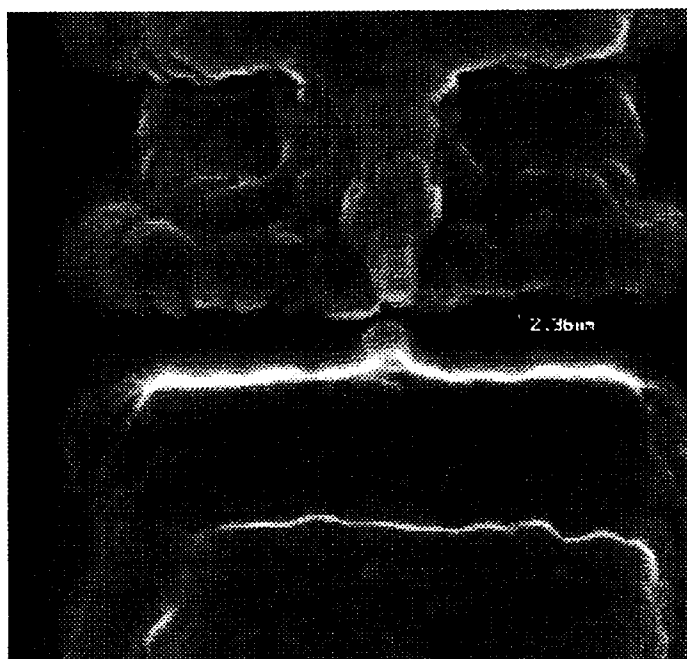


Figure 5. The SEM photo picture of a fabricated closely spaced Al leads with the gap as narrow as 2-5 nm.

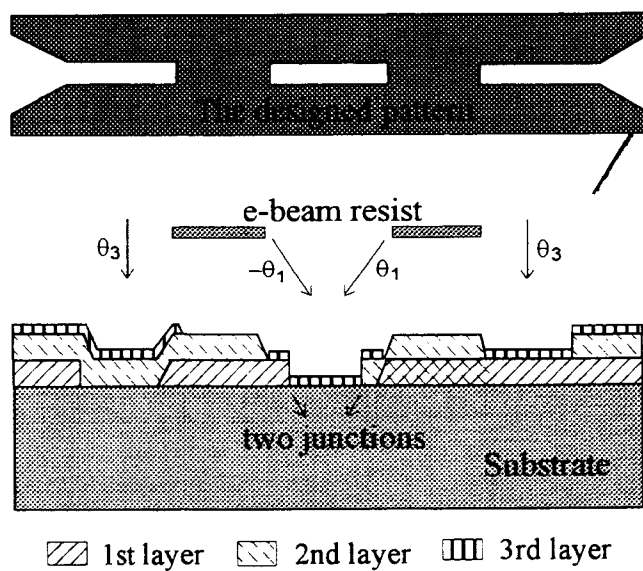


Figure 6. The schematic demonstration of a proposed process for the extension of our SASE technique which may produce smaller junction.