

Low-Temperature Solid-Phase Epitaxy of Defect-Free Aluminum p⁺-doped Silicon for Nanoscale Device Applications

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ABSTRACT

A solid phase epitaxy (SPE) technique was developed to grow p⁺ aluminum-doped crystalline Si in a fully CMOS compatible process. This paper describes the experimental conditions leading to the selective growth of nanoscale single crystals where the location and dimensions are well controlled, even in the sub-100 nm range. The SPE Si crystals are defined by conventional lithography and show excellent electrical characteristics. Fifty-nanometer-thick p⁺ SPE Si crystals were used to fabricate p⁺-n-p bipolar junction transistors. The remarkable control of the whole process, even in the sub-100 nm range, make this module directly usable for Si-based nanodevices.

INTRODUCTION

This work was inspired by the results achieved in the growth of semiconducting nanowires where complex, three dimensional structures have been grown. It is possible to epitaxially grow materials with large lattice mismatches on top of each other in nanowire form since significant strain does not accumulate in small structures. The transitions between the materials are nearly atomically sharp. Another advantage of nanowire growth is that it typically takes place at much lower temperatures than conventional epitaxial growth. Several nanowire growth methods have been developed, such as template-assisted synthesis, laser ablation [1], chemical vapor deposition (CVD) [2], electrochemical deposition [3], and the vapor-liquid-solid (VLS) approach [4-6]. By using these different techniques, a large variety of semiconducting nanowires made of, for example, indium phosphide [7], gallium nitride [8], germanium [9] and silicon [10] have been grown. The most commonly used growth technique is VLS where the nanowires are grown from a vapor-phase Si precursor via a metal catalyst. Due to its physical and chemical properties, gold is frequently used as the catalyst. Gold also has the advantage that it forms eutectic alloys with semiconductor materials at low temperature.

However, not all of these growth techniques are compatible with CMOS technology. Materials such as Au or Fe are not compatible with front-end Si processing because they diffuse and deteriorate the device performance. In addition, the ability to control the dimensions and the position of the nanowires, which is an essential requirement for future IC applications, is not provided by some of the existing growth techniques. Moreover, our results may shed some light on a controversy in the literature concerning VLS growth. K.A. Dick et al. [11] investigated the

growth of III-V nanowires, obtained by metallorganic vapor-phase-epitaxy MOVPE at low-temperature and demonstrated that the metal catalyst never reaches the liquid-phase during the growth sequence. S. Sharma et al. [12] also reported the synthesis of titanium-catalyzed silicon nanowires at temperature of about 600 °C, which is far below the eutectic temperature of Ti/Si alloys, known to be above 1000 °C. These phenomena are not entirely explained by the standard VLS model.

The process described here also proceeds far below the eutectic point and no liquid phase is involved. In a recent paper, we presented a fully CMOS-compatible technique to selectively grow high quality p^+ aluminum-doped silicon elevated contacts and diodes by solid phase epitaxy using an aluminum thin film as a transport medium and amorphous silicon (α -Si) as the silicon source [13]. In the present study, we demonstrate the controllability of the SPE growth in the sub-100 nm range.

EXPERIMENTS

SPE island formation

The sequence of the SPE growth of nanoscale silicon islands in contact windows to Si substrate is illustrated in Fig. 1. A 30-nm-thick layer of silicon dioxide was first thermally grown on a mono-crystalline $\langle 100 \rangle$ silicon substrate. Then a 300-nm-thick low-pressure CVD silicon dioxide (LPCVD SiO_2) was deposited (Fig. 1a) and contact windows were patterned using conventional optical lithography (Fig. 1b). Anisotropic plasma etching through the LPCVD SiO_2 to the thermal oxide was used to obtain contact windows of about 0.7 – 0.8 μm wide.

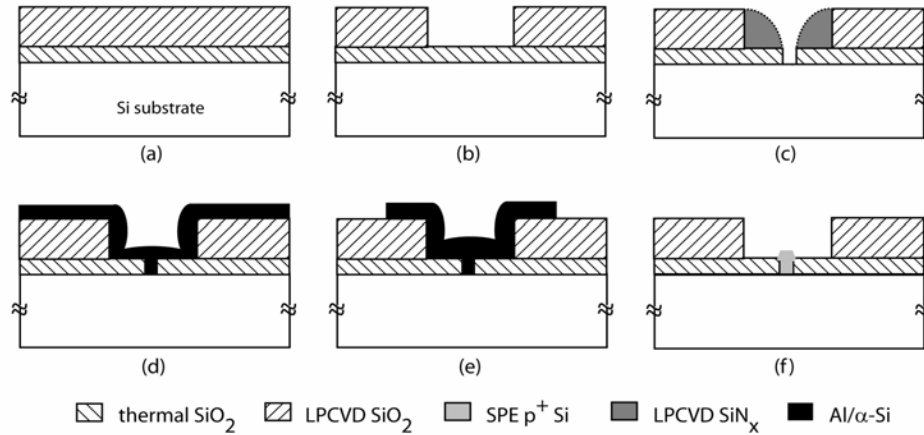


Figure 1. The solid-phase epitaxy sequence. (a) Oxidization (b) Contact window definition (c) SiN_x spacer formation (d) Spacer removal and PVD deposition of Al/ α -Si (e) Al/ α -Si etch definition (f) anneal with transport of α -Si through Al to the c-Si surface. Epitaxial Si observable in the contact windows after Al removal.

The size of the contact windows was then reduced by using silicon nitride (SiN_x) spacers as follows: a 400-nm-thick layer of low-stress LPCVD SiN_x was deposited at 850 °C and anisotropically plasma etched with C_2F_6 to leave spacers of about 350 nm wide. This reduced the width of the contact window mask to the region of 100 nm. The SiN_x spacers served as a hard mask to selectively plasma etch the remaining thermal oxide (Fig. 1c) with a mixture of

C_2F_6/CHF_3 and applying a soft landing on the Si substrate. The native silicon dioxide, mainly induced by the cleaning and etching steps, was removed by dip-etching in HF 0.55% for 4 min before the transfer to the metallization module. A thin layer of aluminum was then deposited from an Al target containing 1% Si by physical vapor deposition (PVD) at room temperature. Optionally, a thin amorphous silicon (α -Si) layer was then deposited in the same PVD system (Fig. 1d). Experiments were performed with and without patterning of this stack (Fig. 1e). Annealing was performed at temperatures between 350 and 500 °C, which is far below the 577 °C eutectic point of the Al/Si alloy. It is a well-known phenomenon in IC-fabrication that the Si in the Al precipitates on the underlying substrate during annealing, with a preference for epitaxial deposition on the c-Si rather than poly-crystallite deposition on the surrounding oxide. For sub-100 nm wide contact windows, enough Si precipitates from a 0.6- μ m-thick Al (1% Si) layer to fill the window. For larger contact windows, our experiments showed that extra Si for filling the windows could be supplied from the sputtered α -Si that, upon annealing, diffuses into the Al. The resulting SPE island is indicated in Fig. 1f, where the Al also has been removed.

The epitaxial growth has been verified by high-resolution transmission-electron microscopy (HRTEM). The results of the HRTEM analysis of the SPE Si crystal/Si substrate interface is presented in Fig. 2. The growth interface is smooth, indicating the silicon native oxide has been dissolved and the epitaxial transition is evident.

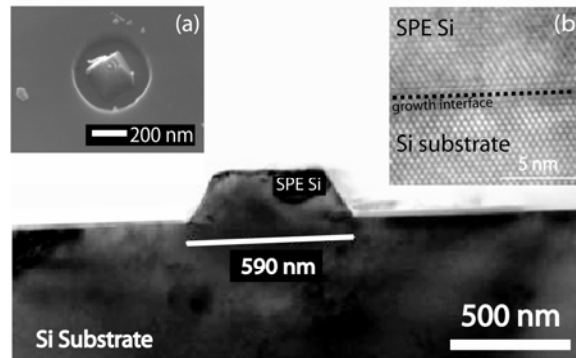


Figure 2. Low-resolution TEM view of a large SPE Si island grown on Si substrate. The contact opening is entirely filled and the crystal facets are visible. The inset (a) represents a SEM micrograph of a sub-100 nm contact window after Si SPE (and Al removal). The scale bar is 200 nm. The inset (b) represents the HRTEM image of the growth interface (dashed line).

Control of SPE island growth

The size of the SPE islands is easily controllable since it is determined by the geometrical parameters of the contact window and the patterned Al/ α -Si layer stack. The growth itself occurs for a large variety of Al thicknesses and the height of the SPE island corresponds to the thickness of the sputtered Al thin film. The control of the position and selectivity of the SPE growth is particularly enhanced by patterning of the Al/ α -Si layer stack before the SPE as shown in Fig 1d. Since the crystal growth, fed from the α -Si layer via a fast diffusion process in the Al layer [14], occurs selectively on the exposed silicon substrate rather than on the surrounding oxide, the patterning of the Al/ α -Si layer stack around the contact window will prevent the diffusion of the Si far away from the contact window and reduce the probability of deposition on the oxide. The influence of the patterned Al/ α -Si layer stack area is examined here more closely by SEM

analysis of large arrays of contact windows with widths from 0.6 to 3 μm surrounded by Al/ α -Si islands with widths from 3 to 11 μm . Initially, the size of the SPE grown crystal increases with the area of the surrounding Al/ α -Si, i.e., when the amount of Si available increases (Fig. 3a, 3b). On the other hand, when the layer stack of Al/ α -Si is patterned in very large islands, the contact windows were found to not be entirely filled and poly-silicon deposition was observed on the surrounding oxide (Fig. 3c). This indicates that, in this situation, a large amount of silicon is consumed by the nucleation of poly-silicon on the oxide, and thus less silicon is available for SPE growth in the contact window. This process may be enhanced by the exposure of the oxide under the Al/ α -Si to plasma and chemicals, producing defaults in the oxide favorable for Si nucleation.

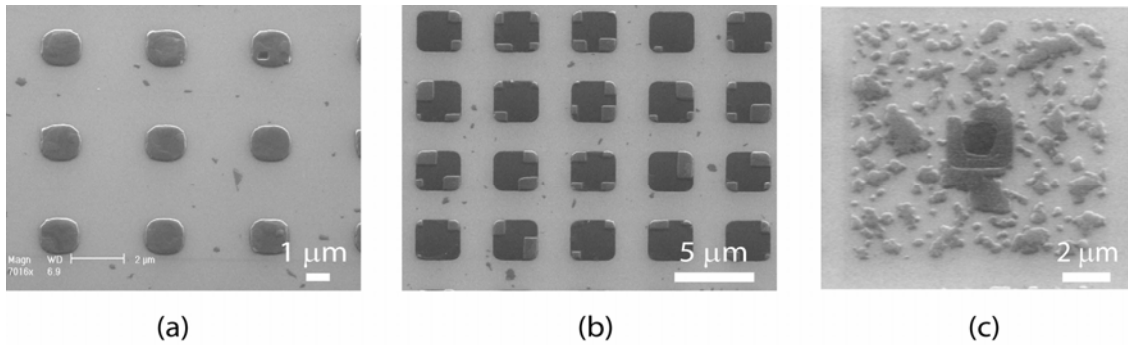


Figure 3. SPE results in the case of (a) the top Al/ α -Si layer patterned in $\sim 5 \mu\text{m}$ wide island around a 1.2- μm -wide contact window. Practically no nucleation on oxide is obtained. (b) insufficient α -Si to entirely fill in a 3- μm -wide contact windows with SPE Si. A selective Si deposition is obtained on the contact window edges. (c) the Al/ α -Si bi-layer patterned in 10 μm large island around a 1.5- μm -wide contact window. A poly-silicon deposition on the oxide is obtained and the contact to Si substrate (black region) is not completely filled in. In all cases, the thicknesses of the Al and α -Si layers were respectively 150 nm and 10 nm.

The SEM-assisted analysis provided the information necessary to determine the optimal ratio between contact-windows size and Al/ α -Si thin-film thicknesses/etch-definition-area for the growth of an SPE island with a desired height and lateral dimensions. An example, obtained for 150-nm-thick Al and 10-nm-thick α -Si layers patterned in 5- μm -wide islands around 1.2 μm wide contact windows, is shown in Fig. 4a. In the case of a bare Si substrate without oxidation and contact windows definition, randomly-localized Si crystals were obtained after the growth sequence, as shown in the Fig. 4b. These SPE islands can then be as large as $5 \times 5 \mu\text{m}^2$.

The contact windows aspect ratio is also an important process parameter since the PVD aluminum deposited at room temperature has very poor step coverage. In order to reduce the aspect ratio before the metal deposition without, at the same time, enlarging the size of the contact openings, the spacers were selectively removed. A dilute solution of H_3PO_4 was used to etch silicon nitride selectively with respect to the thermal oxide and Si substrate. By heating the solution to 157 $^\circ\text{C}$, a selectivity of about 100 was obtained to both materials. In this manner, 90 nm wide contact windows were fabricated and filled with SPE islands, as previously shown in Fig 2a.

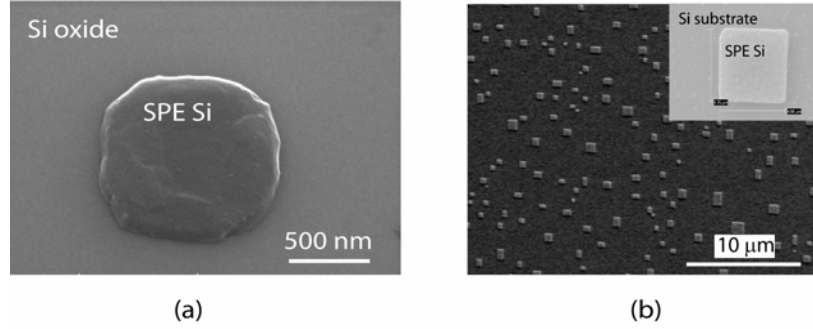


Figure 4. (a) SEM micrograph of an SPE filled $1.2 \times 1.2 \mu\text{m}^2$ contact window. The growth occurs preferably in the exposed Si rather than on the thermal oxide. (b) SEM micrograph of SPE Si crystal growth on bare Si substrate, without contact windows. The inset presents a $\sim 5 \mu\text{m}$ wide SPE Si grown on bare $\langle 100 \rangle$ Si. In both case, the thicknesses of the layer of Al and α -Si were 150 nm and 10 nm, respectively.

SPE Si CHARACTERIZATION

Al Doping

Al-dopants are incorporated during the SPE process so the grown-material is p^+ -doped. A determination of the Al doping level using secondary ions mass spectroscopy (SIMS) has not yet been possible due to the limited analysis area. However, based on contact resistance measurements previously reported [13], the doping of the SPE region is assumed to be, at least, in the order of the reported Al solubility in Si at our process temperatures, i.e. 10^{18} cm^{-3} [15].

Electrical characterization

As reported in [13], the SPE Si was also characterized electrically by fabricating ultra-shallow p^+ -n diodes and p^+ emitters in simple p^+ -n-p bipolar junction transistors (BJTs). Here we present devices with a 25-nm-thick SPE-Si region fabricated with a 30 min anneal in N_2 at 400°C . As shown in Fig. 5, near-ideal diode and BJT characteristics were obtained despite the low-processing temperature, indicating a very low defect-density at the SPE to bulk-Si interface. The saturation current (I_s) of the measured p^+ -n diodes, was found to be $\sim 5 \times 10^{-16} \text{ A}$, which means that the reverse-biased current is below the capability of the measurement equipment.

The abruptness of the doping transition has been verified by capacitance-voltage doping profiling from the substrate to the SPE crystal and these measurements, not presented in this paper, confirm, as it is well known in IC industry, that no Al diffuses into the bulk-Si substrate at temperatures below 500°C .

CONCLUSION

We have demonstrated a reliable technique to fabricate Al-doped SPE grown Si junctions in the sub-100 nm range. The position and dimensions of the SPE deposited island is controlled down to the tens of nanometer range with a thermal budget processing temperature down to 400°C . This makes this process a very promising module for the well-controlled integration of Si based nanodevices in CMOS.

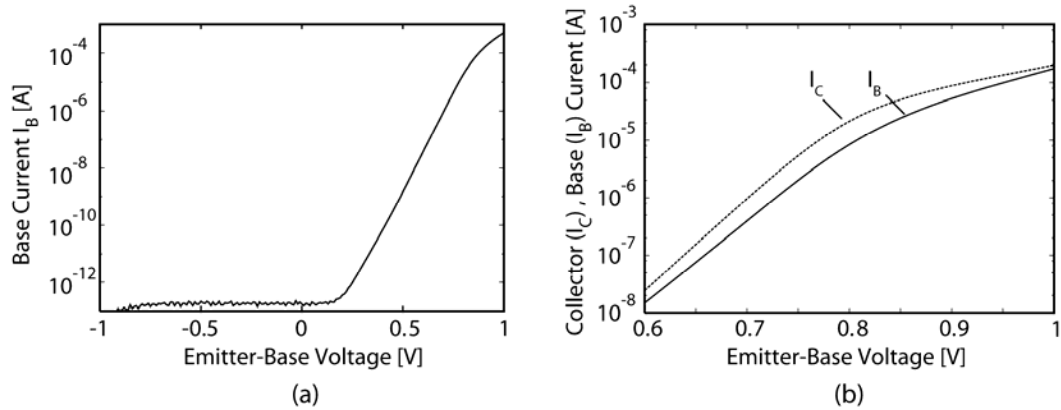


Figure 5. (a) Measured current-voltage characteristic (semi-logarithmic scale) of the emitter-base junction of the fabricated p^+-n-p BJT. The SPE Si emitter is 25 nm thick. (b) Measured forward Gummel plot of a p^+-n-p BJT with a 50-nm-thick and $0.7 \times 0.7 \mu\text{m}^2$ wide SPE p^+ -Si emitter. In both cases, the SPE temperature is 400 °C and the annealing time is 30 min.

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