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Logic circuits based on carbon nanotubes

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Abstract

We demonstrate logic circuits with field-effect transistors based on single carbon nanotubes. A new technique is used for achieving local gates in nanotube field-effect transistors that provide excellent capacitive coupling between the gate and nanotube, enabling the transistor to be ambipolar. The transistors show favorable device characteristics such as a high gain, a large on-off ratio, and room-temperature operation. Importantly, it also allows for the integration of multiple devices on a single chip. Indeed, we demonstrate 1-, 2-, and 3-transistor circuits that exhibit a wide range of digital logic operations such as an inverter, a logic NOR, and an AC ring oscillator.

Keywords: Nanotube; Electronic transport; Logic circuits

The anticipated limits to the further miniaturization of microelectronics have led to intense research directed towards the development of molecular electronics. The use of single-wall carbon nanotubes has stimulated these efforts because these molecules exhibit a range of suitable properties for nanoelectronics. Various basic single-nanotube components have recently been demonstrated, such as molecular wires, diodes, field-effect transistors, and single-electron transistors [1–6]. The next challenge in the development of molecular electronics is to go beyond single-molecule components and integrate such devices onto a chip to demonstrate digital logic operations. Here, we report such logic circuits using single-nanotube field-effect transistors.

The main innovative aspect of our nanotube transistor layout is a local gate that is insulated from the nanotube by a gate oxide layer of only a few nm thickness. Fig. 1a and b show an atomic force microscope image and a schematic cross section of the device, respectively. The gate consists of a microfabricated Al wire with a well-insulating native Al_2O_3 layer that lies beneath a semiconducting nanotube which is electrically contacted to two Au electrodes. This configuration, where the Al_2O_3 thickness of a few nm is much shorter than the separation between the contact electrodes ($\sim$ 100 nm), allows for an excellent capacitive coupling between the gate and the nanotube. Moreover, different local Al gates can easily be patterned such that each one addresses a different nanotube transistor. This layout thus allows the integration of multiple nanotube field-effect transistors (FETs) on the same chip.

Our nanotube circuits are realized in a three-step process. First, Al gates are patterned using electron beam lithography on an oxidized Si wafer. During evaporation, the sample was cooled to liquid nitrogen temperature in order to minimize the roughness of the

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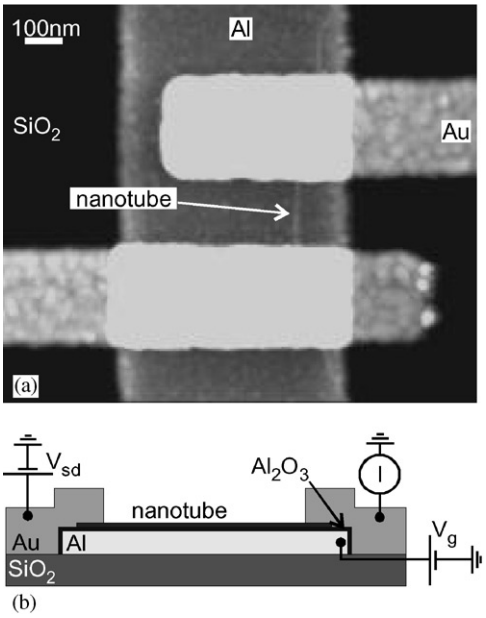

Fig. 1. Device layout. (a) Height image of a single-nanotube transistor, as acquired by an atomic force microscope. (b) Schematic side view of the device. A semiconducting nanotube is contacted by two Au electrodes. An Al wire, which is covered by a few nm thin oxide layer, is used as a gate.

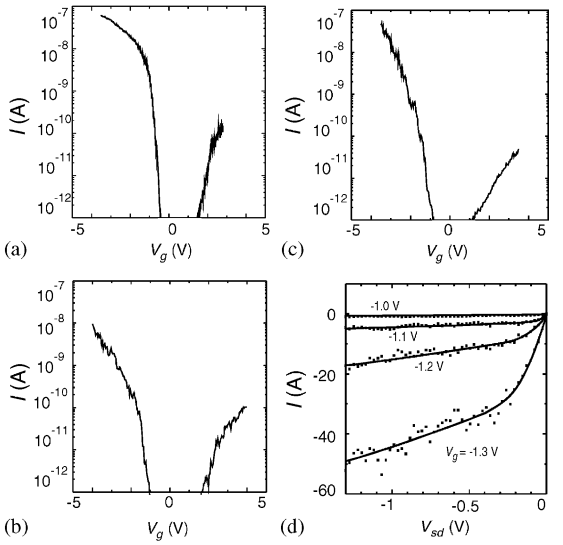

Fig. 2. Room-temperature characteristics of a single nanotube transistor. (a–c) Current as a function of the gate voltage for three different samples. Data were taken at $V_{sd} = 5$ mV in vacuum (about 10^{-4} mbar). (d) $I - V_{sd}$ curves at various values of V_g for a different nanotube transistor. Lines are guides to the eye.

Al surface. The insulator layer consisted of the native oxide that grows by exposing the sample to air. The precise thickness of this layer is difficult to determine, but is on the order of a few nanometers. Capacitance measurements on two large Al films separated by such an oxide layer indicates a thickness of about 2 nm, whereas ellipsometry measurements indicate a value of about 4 nm. Secondly, single-wall carbon nanotubes produced by laser ablation are dispersed on the wafer from a dispersion in dichloroethane. Using an atomic force microscopy, those nanotubes are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires. Their coordinates are registered with respect to alignment markers. Finally, contact electrodes are fabricated with electron-beam lithography by evaporating Au directly on the nanotube without an adhesion layer. The same gold wires serve as interconnect wires that connect the various nanotube FETs.

Fig. 2 shows the device characteristics of a typical nanotube FET. The variation of the current I through the device as a function of the gate voltage V_g (Fig. 2a) shows that both p- and n-type carriers can be injected in the nanotube. Starting from a negative V_g, the current first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion) and finally to the conduction band (inversion) of the semiconducting nanotube. The nearby Al gate thus enables the transistor to be ambipolar. Several volts can be applied on the gate without destroying the oxide layer. This is quite remarkable since the insulator layer is only a few nanometers thin, and it indicates the excellent quality of the gate oxide. The breakdown threshold voltage where the layer is destroyed is typically between 2 and > 4 V. A small gate leakage current (few pA) is observed for V_g approaching such large gate voltages.

Fig. 2b and c show $I(V_g)$ curves for two other samples that have also been measured by sweeping the gate on large voltages. The three curves bare a lot in common. The V_g gap size as well the asymmetry on the p- and n-side are very similar from one sample to the other. These data have allowed us a comparison with a semi-classical model based on Poisson's equation and the study of the non-conventional

screening of charge along the one-dimensional nanotubes [7].

Recently, different groups [8–10] have reported transconductance measurements that also show the injection of both p- and n-type carriers by modifying the gate field. This has been obtained with the "traditional" layout where the gate consists of the Si wafer that is covered by several hundreds of nanometers. Previously, this layout that provides a weaker capacitive coupling between the gate and nanotube has not allowed to inject n-type carriers [5,6]. In order to get n-type carriers, these groups have used new methods such as annealing treatments [9] or the selection of larger diameter nanotubes [10].

Our nanotube transistors can be classified as enhancement-mode p-type FETs because the strongest modulation of the current through the nanotube FET is possible when a negative gate voltage is applied. Fig. 2d shows the current versus bias voltage characteristics. Typical FET-type curves are obtained, with finite currents through the transistor when the gate voltage is more negative than a threshold voltage which is approximately -1.0 V for the current device. In the linear regime at small source–drain voltages, the current is proportional to V_{sd} . In the saturation regime at higher source–drain voltages, that is, when V_{sd} becomes more negative than $V_g - V_t$, the current through the transistor changes more gradually. From the data of Fig. 2 we can extract a transconductance of our nanotube transistors of 0.3 μS, and a lower limit of the on/off ratio of at least 10^5. The maximum current that the nanotube transistor can tolerate is on the order of 100 nA and the on-resistance is 26 MΩ for $V_{sd} = -1.3$ V and $V_g = -1.3$ V. A voltage gain of at least 10 can be achieved. Good contact resistance has been achieved, as is evident from the minimal resistance of 80 kΩ at $V_g = -3.5$ V in Fig. 2a.

To facilitate the comparison of the nanotube transistors to conventional transistors, the data of Fig. 2d were fit to a generic p-type MOSFET model. The model describes the current in the linear regime as $I = -k(1 - wV_{sd})V_{sd}(2(V_g - V_t) - V_{sd})$ and the current in the saturation regime as $I = -k(1 - wV_{sd})(V_g - V_t)^2$. These equations were found to approximate the data well for the parameters $k = 2.3 \times 10^{-7}$ A/V^2, $V_t = -1$ V, and $w = 1$ V^{-1}. While this model provides a reasonable starting point for modeling our devices, a full theoretical description will need to consider the one-dimensional nature and semi-ballistic transport of semiconducting carbon nanotubes.

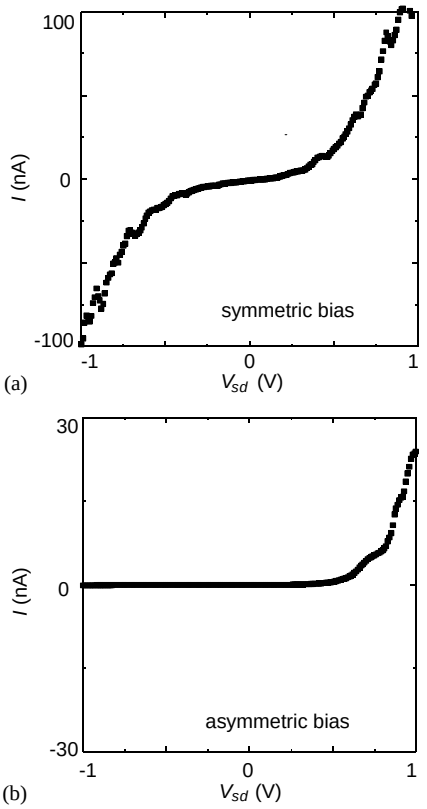

Fig. 3. I–V_{sd} curves of a single nanotube transistor. (a) I–V_{sd} curves under symmetrical bias for $V_g = 0.9$ V. (b) I–V_{sd} curves under asymmetrical bias for $V_g = 0.9$ V.

Fig. 3 shows the $I(V_{sd})$ curves when the nanotube is symmetrically and asymmetrically biased for another sample. For symmetric (asymmetric) bias measurements, the voltages on the Au electrodes are set at $-V_{sd}/2$ and $V_{sd}/2$ (0 and V_{sd}). The curves are dramatically different. For asymmetrically biased nanotubes, the $I(V_{sd})$ curves show asymmetry with respect to the polarity of the bias voltage. Diode characteristics are even obtained for some gate voltage regions (Fig. 3b). Current ratios between 1V and –1V have been measured that are larger than 1000. Symmetrical $I(V_{sd})$ curves are obtained under symmetrical bias (Fig. 3a). Similar results have been obtained on tubes gated by the Si wafer [11]. It has been suggested that this effect comes from the electric field near the contacts that is different in both cases.

It is important to note that the gain is also different from the measurements that are symmetric biased to the one that are asymmetric. The largest gain is obtained for asymmetric biased and for negative voltage measurements as in Fig 2d. This corresponds to curves that are saturating in the current. In the symmetric measurements where there are no saturating currents, lower gains are obtained. However, they are still larger than one, on the order of 4.

A major point of our paper is that small circuits combining these nanotube transistors can be used to make a variety of logic elements. Here we demonstrate an inverter, a NOR gate and a ring oscillator. All of these elements are realized using a logic scheme called resistor-transistor logic. In each of the logic elements, all nanotube transistors were fabricated on a same chip (Fig. 4a). A voltage of -1.5 V across the nanotube was found to be a suitable bias voltage for logic applications. In all logic circuits described here, a voltage of 0 V represented a logical 0 and a voltage of -1.5 V represented a logical 1.

Fig. 4b shows the input–output characteristics of an inverter constructed from a nanotube transistor and an off-chip 100 MΩ bias resistor. An inverter is a basic logic element that converts a logical 0 into a logical 1, and a logical 1 into a logical 0. When the input is a logical 1 ($V_{\text{in}} = -1.5$ V), the negative gate voltage pulls holes into the tube giving it a resistance much lower than the bias resistor. This pulls the output voltage to 0 V, representing a logical 0. When the input of the inverter is a logical 0 ($V_{\text{in}} = 0$ V), then nanotube is nonconducting and the output is pulled to -1.5 V, representing a logical 1. The output voltage of an inverter should make a rapid transition from one logic level to the other as the gate voltage is swept. In this device, the output voltage changes three times faster than the input voltage in the transition region indicating that this particular device has a voltage gain of 3 (other devices showed a gain of up to 6).

A NOR gate can be constructed by simply replacing the single transistor in the inverter with two transistors in parallel (Fig. 4c). The layout of the two transistors on the same chip is shown in Fig. 4a. When either or both of the inputs are a logical 1 ($V_{\text{in}} = -1.5$ V), at least one of the nanotubes is conducting and the output is pulled to 0 V (logical 0). The output is a logical 1 only when both inputs are a logical 0 so that neither nanotube is conducting. In Fig. 4c, the output voltage

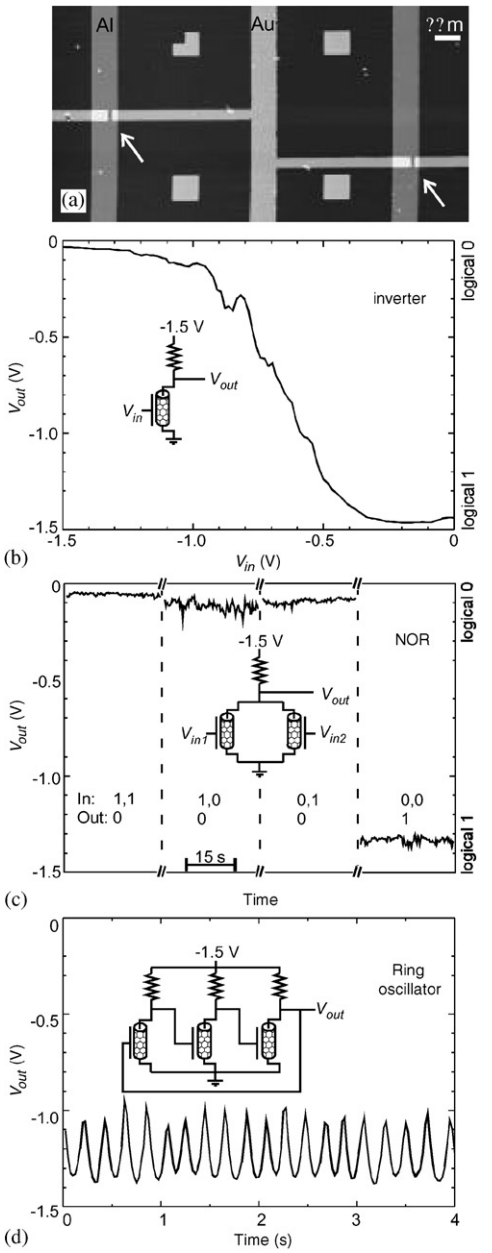

Fig. 4. Demonstration of 1-, 2-, 3-transistor logic circuits with carbon nanotube FETs. (a) Height-mode atomic-force-microscope image of two nanotube transistors connected by a gold interconnect wire. The arrows indicate the position of the transistors. (b) Output voltage as a function of the input voltage of a nanotube inverter. Inset, schematic of the electronic circuit. The resistance is 100 MΩ. (c) Output voltage of a nanotubes NOR for the four possible input states (1,1), (1,0), (0,1), and (0,0). The resistance is 50 MΩ. (d) Output voltage as a function of time for a nanotube ring oscillator. The three resistances are 100 MΩ, 100 MΩ and 2 GΩ.

is plotted as a function of the four possible input states (0,0), (0,1), (1,0), and (1,1), verifying that this circuit indeed operates as a NOR gate. Using variations of the device circuitry one can realize any logical gate (AND, OR, NAND, XOR, etc.) in this way.

A 3-transistor device was realized in the ring oscillator shown in Fig. 4d. This circuit, used to generate an oscillating AC voltage signal, was built by connecting three inverters in a ring. A ring oscillator has no statically stable solution and the voltage at the output of each inverter consequently oscillates as a function of time. One of the inverter outputs is plotted in Fig. 4d. A clear voltage oscillation is observed. The oscillations of 5 Hz frequency were determined by the output impedance of the inverters ($\sim$ 1 GΩ) and the capacitance of the output nodes which currently is dominated by $\sim$100 pF parasitic capacitance of the wires connecting to the off-chip bias resistors.

This paper reports the realization of digital logic with nanotube FET circuits, which represents an important next step towards nanoelectronics. Very recently, other groups have reported the demonstration of circuits incorporating molecular-scale components. Derycke et al. [12] and Liu et al. [13] have built an inverter circuit from chemically doped nanotubes. Huang et al. [14] demonstrated several circuits using semiconducting nanowires that are assembled with microfluidics tools. Schön et al. [15] also demonstrated an inverter based on small organic molecules. These different reports have used very different techniques and molecules to achieve a circuit. This shows that the field is progressing rapidly and is very encouraging for future advances in molecular electronics.

References

[1] S.J. Tans, et al., Nature 386 (1997) 474.
[2] M. Bockrath, et al., Science 275 (1997) 1922.
[3] Z. Yao, H.W. Ch. Postma, L. Balents, C. Dekker, Nature 402 (1999) 273.
[4] M.S. Fuhrer, et al., Science 288 (2000) 494.
[5] S.J. Tans, A.R.M. Verschueren, C. Dekker, Nature 393 (1998) 49.
[6] R. Martel, T. Schmidt, H.R. Shea, T. Hertel, Ph. Avouris, Appl. Phys. Lett. 73 (1998) 2447.
[7] A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker, Science 294 (2001) 1317.
[8] J. Park, P.L. McEuen, Appl. Phys. Lett. 79 (2001) 1363.
[9] R. Martel, et al., Phys. Rev. Lett. 87 (2001) 256805.
[10] A. Javey, M. Shim, H. Dai, Appl. Phys. Lett. 80 (2002) 1064.
[11] C. Zhou, J. Kong, H. Dai, Appl. Phys. Lett. 76 (2000) 1597.
[12] V. Derycke, et al., Nano Lett. 1 (2001) 453.
[13] X. Liu, C. Lee, C. Zhou, J. Han, Appl. Phys. Lett. 79 (2001) 3329.
[14] Y. Huang, et al., Science 294 (2001) 1313.
[15] J.H. Schön, H. Meng, Z. Bao, 413 (2001) 713.