# Sub-500 °C Solid-Phase Epitaxy of Ultra-Abrupt p<sup>+</sup>-Silicon Elevated Contacts and Diodes

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Abstract—A well-controlled low-temperature process, demonstrated from 350 °C to 500 °C, has been developed for epitaxially growing elevated contacts and near-ideal diode junctions of Aldoped Si in contact windows to the Si substrate. A physical-vapor-deposited (PVD) amorphous silicon layer is converted to monocrystalline silicon selectively in the contact windows by using a PVD aluminum layer as a transport medium. This is a solid-phase-epitaxy (SPE) process by which the grown Si is Al-doped to at least  $10^{18}~\rm cm^{-3}$ . Contact resistivity below  $10^{-7}~\Omega \cdot \rm cm^2$  is achieved to both p $^-$  and p $^+$  bulk-silicon regions. The elevated contacts have also been employed to fabricate p $^+$ -n diodes and p $^+$ -n-p bipolar transistors, the electrical characterization of which indicates a practically defect-free epitaxy at the interface.

*Index Terms*—Al-doping, elevated contacts, low-ohmic contacts, low-temperature processing, p-n-p bipolar junction transistors, solid-phase epitaxy, ultra-shallow junctions.

# I. Introduction

HIS LETTER presents a process that can be performed from 350 °C to 500 °C, for fabricating epitaxially deposited p<sup>+</sup> Si islands in contact windows to a monocrystalline Si (c-Si) substrate. The deposition mechanism is a solid-phase epitaxy (SPE) process: the contact window to the c-Si substrate is covered by a layer-stack of thin Al and amorphous Si  $(\alpha$ -Si) and a furnace anneal initiates the transport/epitaxy of the latter at temperatures far below the 577 °C eutectic point of the Al/Si alloy. The SPE of Si from Al/Si has been first reported in the early years [1]–[3], and more recently, similar mechanisms have been proposed to explain the growth of semiconducting nanowires catalyzed by Au [4] and the formation of polycrystalline-Si islands for solar cells using comparable process schemes [5]. The present letter is the first demonstration of i) a very well-controlled process for fabricating Al-doped p<sup>+</sup> elevated contacts and of ii) the incorporation of these regions in Si devices, more specifically p<sup>+</sup>-n diodes and p<sup>+</sup>-n-p bipolar transistors. The electrical characterization of these devices over the wafer, wafer to wafer, and run to run, shows that the process reliably gives nearly-ideal diode characteristics. This

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confirms, as supported by transmission electron microscopy (TEM) analysis, that this is a practically defect-free epitaxy process. Additional noteworthy properties are a low contact resistivity and an ultra-abrupt p<sup>+</sup>-p or p<sup>+</sup>-n doping transition. These properties make this SPE process attractive for backend processing (e.g., post-metallization add-on contacts and diodes) as well as for front-end device processing (e.g., the p<sup>+</sup>-p structure is directly applicable for source/drain contacting in PMOS transistors and p<sup>+</sup>-n diode is applicable for base contacting in SiGe n-p-n HBTs and for emitter formation in SiGe p-n-p HBTs). In all these devices, the low SPE formation temperature means that the transient-enhanced diffusion of the already doped layers can be avoided [6].

# II. EXPERIMENTS

The process flow is shown in Fig. 1. Contact windows in a thermal-oxide isolation layer are etched with HF to the  $\langle 100 \rangle$  Si substrate. Just before metallization, the native oxide is removed by 4 min HF 0.55% dip-etch. The room-temperature physical vapor deposited (PVD) layer stack of Al (containing 1% Si) and  $\alpha$ -Si is deposited without breaking vacuum. The SPE is successfully induced by thermal annealing in a nitrogen vacuum for temperatures down to 350 °C and occurs for a variety of different ratios of Al to  $\alpha$ -Si thickness. The electrical measurements reported below are limited to a combination of 30-nm thermal-oxide isolation, 100-nm Al, 10-nm  $\alpha$ -Si, and a 30-min anneal at 500 °C. The crystal-growth process is controlled by patterning the Al/ $\alpha$ -Si stack in islands around the contact window [Fig. 1(b)]. The c-Si precipitates are then preferentially initiated in the corners of the contact windows [Fig. 1(c)], presumably due to a stress driven process. For window sizes below  $2 \times 2 \mu m^2$ , the window filling is apparently so fast that the first precipitate to form fills the window. The subsequent crystal growth is fed from the  $\alpha$ -Si layer via a fast diffusion process in the Al [7]. Upward crystal growth stops abruptly when the crystal protrudes above the 100-nmthick Al layer [Fig. 1(d)]. Lateral growth proceeds until the contact window is filled [Fig. 1(e)]. The epitaxial growth is seen in the TEM analysis of the growth interface shown in Fig. 2.

## III. DEVICE FABRICATION AND CHARACTERIZATION

The contact resistance to both  $p^-$  (doping down to  $10^{15}~{\rm cm}^{-3}$ ) and  $p^+$  bulk-silicon regions was found to be low ohmic in all cases and the total contact resistivity of the elevated contact plus metallization was measured to be at most

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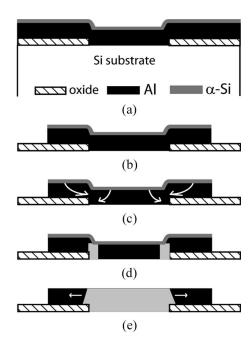


Fig. 1. The SPE sequence. (a) Contact window definition and Al/ $\alpha$ -Si PVD deposition. (b) Al/ $\alpha$ -Si etch definition. (c) Anneal with transport of  $\alpha$ -Si through Al to the c-Si surface. (d) Crystal growth initiates at window corners and edges. (e) Vertical crystal growth stops when the crystal protrudes above the Al and lateral growth then predominates.

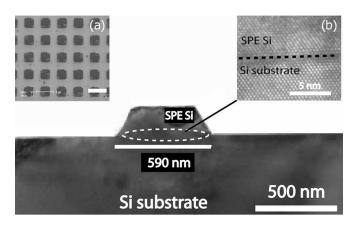


Fig. 2. Cross-sectional TEM image of SPE  $p^+$  Si island showing the Si crystal facets. The inset (a) is an SEM micrograph (after wet Al removal) of the initial stages of SPE. In these larger windows, the initiation of crystallization in the corners is evident. The scale bar is 5  $\mu$ m. The inset (b) is a high-resolution TEM (HRTEM) of the interface with the Si substrate demonstrating the epitaxial growth.

 $10^{-7}\Omega\cdot\text{cm}^2$  [Fig. 3(a)], which confirms that the SPE Si is highly p-doped with Al. In accordance p<sup>+</sup>-n diodes are formed on n-Si, the I-V characteristics of which are near-ideal with an ideality factor of 1.02 [Fig. 3(b)]. The correspondingly low leakage current indicates a very low density of generation/recombination centers in the depletion region that only can be achieved by an exceptionally low defect-density at the growth interface where the metallurgic junction also is positioned. For non-elevated contact windows, an Al to n-Si Schottky diode is formed that has a two-decades-higher saturation current. The high quality and controllability of the SPE-Si regions are particularly well monitored when they are used as emitters in simple p<sup>+</sup>-n-p transistors (Fig. 4). Near-

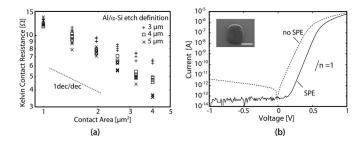


Fig. 3. (a) Contact resistance of SPE p<sup>+</sup> filled contacts measured on special Kelvin test structures with low-ohmic p<sup>+</sup> diffusion taps [8]. The measured resistance includes the resistance through the SPE Si region that is wider for larger Al/ $\alpha$ -Si etch definition, i.e., the resistance decreases when the latter increases. (b) I-V characteristics of  $1 \times 1~\mu$ m<sup>2</sup> junctions fabricated on 2–5  $\Omega$ -cm n-type substrate. The solid line is for a SPE p<sup>+</sup>-n diode and the dashed line for an Al/Si (1%) Schottky diode. The inset shows a SEM micrograph of SPE filled  $1.2 \times 1.2~\mu$ m<sup>2</sup> contact window (the scale bar is  $1~\mu$ m).

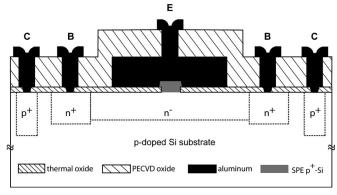


Fig. 4. Schematic cross section of the p<sup>+</sup>-n-p bipolar junction transistor in which the emitter is deposited by SPE. The base doping is  $2\times 10^{17}~\text{cm}^{-3}$ .

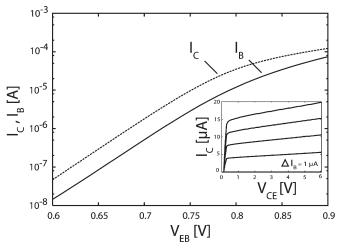


Fig. 5. Measured Gummel plot of a representative p<sup>+</sup>-n-p with an emitter area of  $1\times 1\,\mu\mathrm{m}^2$  and the current gain about 3.5. In the ideal region for  $V_{\mathrm{EB}}=0.6$  V, the over-the-wafer-measured base current is  $I_B=16\pm 2.8$  nA  $(2\sigma)$ . The  $I_B$  is directly function of the SPE dependent parameters (such as thickness, width, and doping of the grown p<sup>+</sup> Si) but the influence of the pre-SPE process steps (e.g., lithography, wet chemical over-etch) are also included in the given spread. The inset shows the corresponding output characteristics.

ideal forward base and collector currents are obtained with a current gain of  $\sim 3.5$ . Particularly, the extremely good uniformity of the base current over the wafer and from run to run confirms that the p<sup>+</sup>-emitter thickness and doping over the wafer is very reproducible (Fig. 5). The solid solubility

of Al in Si at 500 °C reported in literature when implantation plus thermal activation is used is about  $3\times10^{18}$  cm<sup>-3</sup> [9]. In the SPE process, dopant incorporation is achieved during growth and higher doping levels are expected. The very low contact resistivity and inspection of the island surface along with secondary ions mass spectroscopy (SIMS) of a small area including an SPE island (not shown in this paper) indicate that the surface of the grown Si is very highly Al doped. However, a quantitative doping profile measurement on only the grown-Si has not yet been possible due to the limited island size.

### IV. CONCLUSION

The SPE  $p^+$  elevated contacts demonstrated in this letter have several remarkable properties considering that the processing temperature can be as low as 350 °C. Indeed, for all fabricated devices ( $p^+$ - $p^-$  and  $p^+$ - $p^+$  contacts,  $p^+$ -n diodes and  $p^+$ -n-p bipolar transistors), the electrical characterization showed clearly that very controllable growth conditions have been found whereby the contact window was entirely filled with an exceptionally low defect-density at the interface with bulk-Si. The thickness of the elevated contact was highly reproducible, uniform, and determined by the original Al-layer thickness that was, in some cases, only 25-nm thick. Moreover,

an attractively low contact resistivity of less than  $10^{-7}~\Omega\cdot\text{cm}^2$  was reproducibly achieved.

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