

AN OFFSET-CHARGE INDEPENDENT SINGLE-ELECTRONICS RS FLIP-FLOP

P. HADLEY, E. H. VISSCHER, Y. CHEN, and J. E. MOOIJ

*Applied Physics, Delft University of Technology
Lorentzweg 1, 2628 CJ Delft, The Netherlands*

Single-electronics circuits can detect charges much smaller than the charge of an electron. This enables phenomenally precise charge measurements but it also means that charged defects (often referred to as offset charges) can disrupt device operation. It has been suggested that large scale integration of single-electron devices could be used to construct fast logic circuits with a high device packing density. In small circuits, the offset charges are tuned away by applying voltages to a number of gates. In large circuits, it is impractical to tune the offset charges by coupling a gate to every device. Since the complete elimination of offset charges is probably impossible, offset-charge independent circuits must be developed. Here an offset-charge independent RS flip-flop is described. This circuit is equivalent to a static RAM memory cell. Although the flip-flop is offset-charge independent, it does occasionally forget the information that was stored in it.

1. Introduction

Single electron tunneling (SET) devices can be used to construct circuits which process information by manipulating individual electrons. The general characteristics of SET devices are that they are small, dissipate little power, and can detect exquisitely small quantities of charge. The small size and low power dissipation of SET circuits makes them potentially useful for the information technology industry. The possible applications of SET circuits have been detailed in a number of review articles.¹⁻³ These reviews also identify a number of challenges that the SET community must overcome if SET circuits are ever to have any practical application. Among the practical problems are the necessity for low temperature operation and the inevitable random offset charges. The path that must be followed to make circuits that operate at higher temperatures is clear; the dimensions of the devices must be reduced. In the last few years there has been considerable progress in fabricating smaller devices. The issue of offset charges is more subtle and less progress has been made. An important contribution to offset-charge independent circuits was made by Likharev and Korotkov who described an offset-charge independent DRAM cell.⁴ In this paper, the

general trends in single electronics will first be sketched and then another offset-charge independent memory cell will be described.

2. Trends in Single Electronics

There has been steady progress in reducing the dimensions of SET circuits. A large international effort in nanofabrication is underway that will eventually make molecular-scale devices a reality. When SET circuits are scaled down to molecular dimensions, they will function at room temperature. This shrinking of the circuit dimensions has a number of consequences both desirable and undesirable. As the size and the capacitance of the devices decrease, the operating temperature, the operating voltage, and the device packing density increase. These are desirable consequences of the shrinking of SET devices. However, as the dimensions decrease, the electric fields, the current densities, the energy dissipated per switching event, and the power dissipated per unit area all increase. These are undesirable consequences of shrinking.

Table I shows how the various parameters for single electronics and CMOS⁵ scale as the dimensions of the devices are decreased by a factor of α . Here it is assumed that the lateral dimensions of the SET devices are determined by the gate capacitor. The gate capacitance must be larger than the junction capacitance to ensure that the SET transistors have gain. This implies that the gates must be physically the largest components of SET devices and they therefore determine the device packing density. As the circuits are scaled down, the capacitances scale as $1/\alpha$ and the device density increases as α^2 .

The energy required to move an electron in a SET circuit is the charging energy,

Table I. The scaling of various parameters of SET circuits and CMOS as the dimensions of the devices are decreased by a factor of α . For CMOS, constant electric field scaling is used.

	Single Electronics	CMOS
Operating Frequency	α	α
Operating Temperature	α	--
Voltage Level	α	$1/\alpha$
Electric field	α	1
Packing density	α^2	α^2
Power dissipated/device	α^2	$1/\alpha^2$
Power density	α^4	1

$E_C = e^2/(2C_\Sigma)$, where C_Σ is the characteristic capacitance of the device. The charging energy is approximately the energy dissipated when a SET device switches. The charging energy, the operating temperature $\propto e^2/(2k_B C_\Sigma)$, and the voltage level $\propto e/C_\Sigma$, all scale like α . The operating frequency also scales with α , $\propto 1/(RC_\Sigma)$. This assumes that C_Σ is greater than the interconnect capacitances. When C_Σ is smaller than the interconnect capacitance, this scaling no longer holds and the product of the SET resistance and the interconnect capacitance determines the speed of the devices. The dissipated power density is proportional to the energy dissipated per switching event times the operating frequency times the device density. Thus the power density scales like α^4 . A large dissipated power density is undesirable yet it grows faster than all of the other parameters as the SET circuits are scaled down. Notice that while the voltage level and the power dissipated per device are decreasing as CMOS is scaled down, they are increasing as SET circuits are scaled down. In terms of power dissipation, the two technologies are moving towards each other.

3. The RS flip-flop

An RS flip-flop is a device that has two stable states. These two states can be used to store information. In this relatively simple circuit, many of the problems common to larger SET circuits are confronted. In order to construct a flip-flop, wires must cross, gain is required, offset charges must be regulated, and parasitic capacitances must be considered. A flip-flop is generally constructed by taking two inverters and connecting the output of each inverter to the input of the other inverter. (See Fig. 1a.) This two inverter circuit has two stable solutions: the output of the first inverter can be low while the output of the second inverter is high or the output of the first inverter can be high while the output of the second inverter is low. When a flip-flop is used as a memory cell, the two stable states represent a zero and a one. In that case, the RS flip-flop is also called a static RAM or SRAM cell.

A SET inverter that could be used to build a flip-flop is illustrated in Fig. 1b.^{6,7} The offset charges, q , of the two SET transistors that make up the inverter have been specified in the drawing. If the offset charges are not known, then the output of the inverter cannot be determined by knowing the input of the inverter. However, if two such inverters are coupled to form a flip-flop, it is possible that information that was written to the flip-flop can be recovered without knowing the values of any of the four offset charges. To understand how this is possible we consider the operation of the flip-flop.

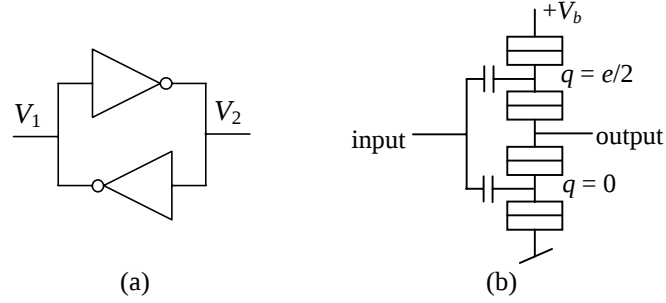


Fig. 1 (a) The schematic of an RS flip-flop constructed by coupling two inverters. (b) A SET inverter realized with tunnel junctions. The offset charges q are specified to insure proper inverter operation.

The state of the flip-flop is specified by the two output voltages V_1 and V_2 . (See Fig. 2.) The values of the output voltages are determined by the bias voltage, the offset charges, and the initial state of the circuit. Depending on the values of the offset charges, there can either be one stable solution for the output state or two stable solutions and one unstable solution. When information is written to the flip-flop, an external agent pulls one of the outputs high and the other output low. The external agent then releases the outputs of the flip-flop and they evolve towards some steady state solution. If the offset charges are such that there is only one stable solution, then the flip-flop evolves to that state and all knowledge about the initial state is lost. In this case the memory cell forgets the information that was written to it. The information is not lost if the offset charge configuration is such that the circuit is

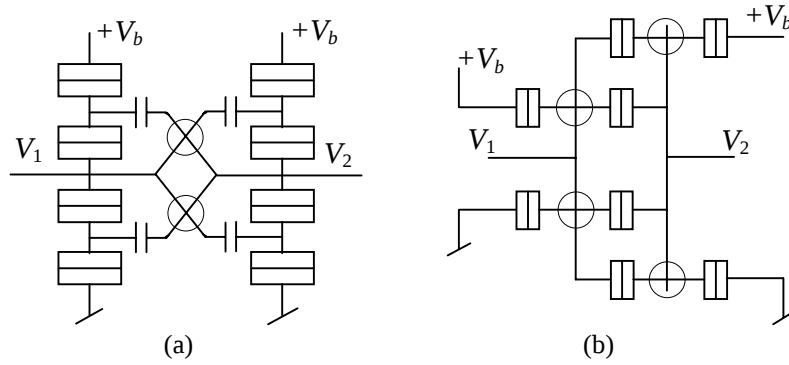


Fig. 2 (a) The schematic of an RS flip-flop constructed by coupling two SET inverters. The circles indicate the points where wires cross in the circuit. In this case, the capacitors formed where the wires cross is an undesirable parasitic. (b) The same flip-flop circuit realized with another layout. The points where the wires cross capacitively couple elements that need to be coupled for the proper functioning of the circuit. No undesired parasitic capacitances are generated in this layout.

bistable. Then when the external agent releases the circuit, it evolves to the stable solution that is closest to the initial state. Simulations show that if information is written to a collection of such flip-flops with random offset charges, a correct bit is retrieved 53% of the time. This is a very forgetful memory cell. It barely outperforms a device that returns random bits and the correct bit is returned 50% of the time. The reason the flip-flop performs so poorly as a memory cell is that bistability only exists for a narrow range of offset charges. When the device is bistable it works; when there is only one solution, it does not work.

One way to improve the performance of the flip-flop is to construct a circuit that always has multiple stable solutions irrespective of the value of the offset charges. The existence of multiple solutions is a generic property of coupled nonlinear elements. Many SET circuits could be devised which have this property. An example of such a circuit is shown in Fig. 3. Here eight SET transistors are coupled together to form a RS flip-flop. When this circuit is released from its initial state it evolves to the nearest stable solution thus preserving information about the initial state. In simulations with $C_g = 2C_j$, $C_\Sigma = C_g + 2C_g$, $V_b = e/C_\Sigma$, and a random distribution of offset charges, this cell returned the correct bit 97% of the time. Here C_g is the gate capacitance, C_j is the junction capacitance, and V_b is the bias voltage.

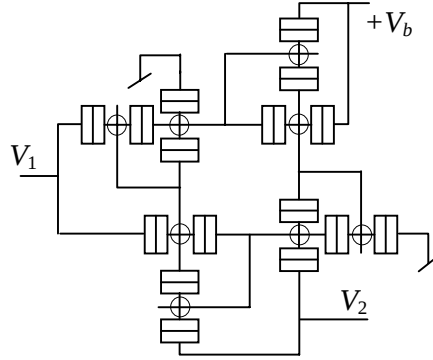


Fig. 3. An RS flip-flop fabricated from eight SET transistors. The circles highlight overlap capacitors formed where two wires cross. No undesirable parasitic capacitances are formed.

Conclusions

The scaling of various parameters of SET circuits was considered as the circuits are scaled down. It was found that although there are desirable consequences of decreasing the circuit size, there are also undesirable consequences. In particular, the dissipated power density increases dramatically as SET devices are scaled down. Parasitic capacitances also play a more important role when the circuits are scaled down. Layouts that eliminate the formation of undesirable parasitic capacitances are shown in Fig. 2 and Fig. 3. It was argued that SET circuits with multiple stable solutions could be used as memory cells irrespective of the values of the offset charges in these circuits. An example of such a circuit is shown in Fig. 3. Simulations show that such memory cells with random offset charges return the correct bit 97% of the time.

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