

Fabrication of multilayer single-electron tunneling devices

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A reliable process has been developed for the fabrication of multilevel single-electron tunneling (SET) devices. Using this process, we have fabricated SET devices with Au-SiO-Al and Al-AlO_x-SiO-Al overlap capacitors. The SET transistors exhibit voltage gain and, despite the complex device structure, have a low charge noise ($7 \times 10^{-5} e/\sqrt{\text{Hz}}$). Moreover, the use of overlap capacitors in SET devices results in a reduction of cross capacitances down to 8%. © 1995 American Institute of Physics.

Recent advances in nanolithography have led to the development of single-electron tunneling (SET) devices. The basic building block of these devices is the SET transistor.¹ A SET transistor consists of a small metallic island coupled to three terminals. A gate is coupled to the island by a capacitor and the output terminals are coupled to the island by tunnel junctions. The capacitance of the island is so small that the addition of just one electron to the island significantly changes the electrostatic energy of the island. This leads to a phenomena called the Coulomb blockade.² The Coulomb blockade suppresses current flow between the two output terminals for all voltages below a certain threshold voltage. This threshold voltage is a periodic function of the charge on the gate with a periodicity of the elementary charge of an electron, e . SET transistors have already been used to measure the motion of single electrons in the electron box^{3,4} and the charge trap.⁵ Such measurements would be impossible with commercial electrometers. Other SET devices take advantage of the discreteness of charge to perform digital functions. The electron turnstile⁶ and the electron pump,⁷ are used to establish precise currents where single electrons are transferred one by one through the device. By doing this repeatedly with frequency f , a constant current can be generated with a value $I = ef$. Families of SET logic have also been proposed. The Coulomb blockade and SET devices have been described in detail in a number of review articles.⁸

Until now, SET devices have been fabricated in one single lithographic step, using a shadow evaporation technique.⁹ In this step, tunnel junctions, coplanar or overlap capacitors,¹⁰ and resistors¹¹ have to be fabricated. In this paper we present a multilayer fabrication process, in which different layers are aligned on top of each other very accurately. We have applied this process to the fabrication of SET devices with overlap capacitors in which the metallic base electrodes, the dielectric, and metallic islands with tunnel junctions are processed independently. Despite the more complicated device structure, the fabricated SET transistors exhibit low charge noise characteristics. The use of the compact geometry of the overlap capacitors results in a significant reduction of undesirable cross capacitances from gate electrodes to the neighboring metallic islands.

SET devices with either Au-SiO-Al or Al-AlO_x-SiO-Al thin film overlap capacitors have been fabricated. The circuits were fabricated on Si substrates which have a 0.5 μm

thermally oxidized SiO₂ top layer to reduce stray capacitances to ground. Each layer required four basic fabrication steps of resist baking, e -beam writing, material deposition, and lift-off. The layers were aligned on top of each other with a set of Au markers within an accuracy of 20–30 nm using a Philips EBPG HR-5 e -beam writer. The first layer of the Au-SiO-Al SET was a 40-nm-thick Au pattern which defined the base electrodes of the gates. On top of the Au pattern, we deposited a 100-nm-thick amorphous SiO layer which formed the dielectric of the overlap capacitor. The dielectric was deposited using e -beam evaporation at a rate of 10 Å/s, a substrate temperature of 10 °C, and a base pressure of 10^{-7} Torr. The third layer formed the Al island and the two Al-AlO_x-Al tunnel junction of the SET device. The junctions were fabricated by a two angle shadow evaporation⁹ using a double layer PMMA/MAA-PMMA shadow evaporation mask. The thicknesses of the aluminum layers were 30 and 70 nm. The Al-AlO_x-SiO-Al SET devices were fabricated using the same process except that an *aluminum* base electrode was used which was thermally oxidized for 3 h at a temperature of 300 °C. Afterwards, a 50 nm SiO layer was deposited resulting in a larger gate capacitance without changing the geometry of the metallic island.

Figures 1(a) and 1(b) show scanning-electron micrographs of two capacitively coupled SET transistors and a six-junction series array with overlap capacitors. Figure 1(c) shows the schematic circuit of a SET transistor. The small metallic island is connected to two tunnel junctions with capacitances C_1 and C_2 and tunnel resistances R_1 and R_2 . An external voltage, V_g , can induce a charge, $Q = V_g C_g$, on the island via the gate capacitor C_g . The island has a total capacitance of $C_\Sigma = C_1 + C_2 + C_g$. When current biased, the output voltage V_o , is periodic in the gate voltage with a period of $\Delta V_g = e/C_g$. For certain bias currents, the $V_o - V_g$ curves form a sawtooth pattern which has slopes of $C_g/(C_g + C_1)$ on one side and $-C_g/C_2$ on the other. The theoretical voltage gain is $K_V = C_g/C_2$ and can be greater than unity if $C_g > C_2$. We deduced the device parameters by fitting the experimental data to the theoretical $V_o - V_g$ curves derived from the orthodox theory^{2,12} without taking cotunneling into account.¹³ All measurements were performed in a dilution refrigerator with a base temperature of 10 mK. Special care was taken to reduce the noise reaching the SET device. In particular, all leads down to the sample had special

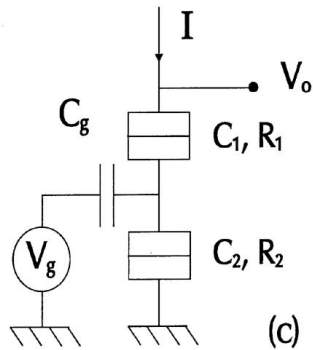
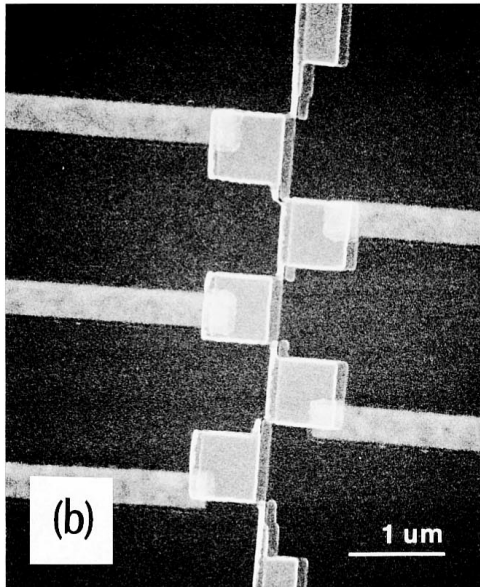
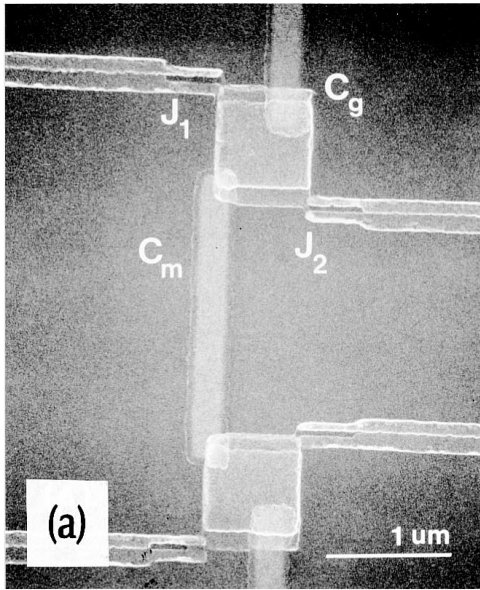


FIG. 1. (a) Scanning electron micrograph of two capacitively coupled SiO SET transistors. The tunnel junctions J_1 and J_2 are defined by the overlap of the horizontal leads and the square metallic island. Both islands have a overlap gate C_g , and are coupled to each other by a vertical coupling capacitor C_m . In (b), a six junction series array is shown. Each square metallic island is coupled to a horizontal overlap gate via a SiO dielectric. The schematic circuit of a current biased SET is shown in (c). The tunnel junctions are indicated by boxes.

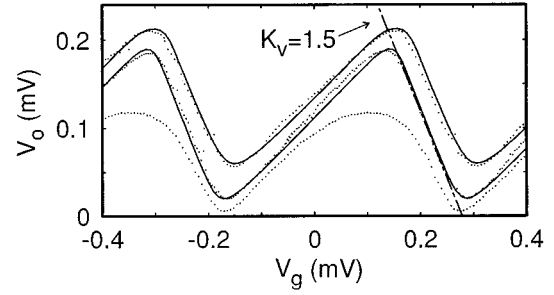


FIG. 2. Output voltage as a function of the gate voltage at fixed bias currents of a Al-AlO_x-SiO-Al SET transistor. The bias currents are 1, 26, and 50 pA. The solid lines indicate the best fits to the experimental data at moderately high bias currents. A maximum attainable voltage gain of 1.5 is indicated by the dashed line.

high-frequency copper powder filters.¹⁴ A magnetic field of 2 T was applied to keep the aluminum in the non-superconducting state.

In Fig. 2, the results of the Al-AlO_x-SiO-Al SET transistor are shown. By fitting the data we obtain, $R_1=210$ k Ω , $R_2=200$ k Ω , $C_1=0.21$ fF, $C_2=0.20$ fF, and a device temperature of 60 mK. The 200×200 nm² gate capacitor has a capacitance of 0.36 fF. The experimental voltage gain is $K_V=1.5$, as indicated by the dashed line in Fig. 2, and is slightly less than the theoretical maximum voltage gain of $K_V=1.8$, calculated from the device parameters. This can be attributed to thermal heating of the device due to power dissipation and insufficient filtering of the leads. The Au-SiO-Al SET transistor has similar device parameters except for a gate capacitance of 0.12 fF. Using the parallel-plate formula, we estimate a geometrical capacitance of 0.03 fF for the 100-nm-thick SiO overlap gate, using $\epsilon_r=4$ for the SiO dielectric. The discrepancy between the geometrical estimation and the measured value is most likely due to the edges and SiO step coverage of the gate which consequently results in an increased effective capacitance.

We have also tested whether a SET device could withstand a full fourth fabrication cycle in which we locally deposited a 100-nm-thick SiO layer on top of the Au-SiO-Al SET transistor. The device did not show any significant parameter change after processing. This opens the possibility that SET devices can be integrated in different layers in the same circuit.

We determined the quality of the SET transistors by measuring their $1/f$ (Ref. 15) noise spectrum. The charge noise of the Au-SiO-Al SET transistor was measured, operating the device in a charge locked loop similar to the flux locked loop of a dc SQUID.¹⁶ Figure 3 shows the measured input charge noise Q_N and the related energy sensitivity $E_N=Q_N^2/2C_\Sigma$ as a function of the frequency. The energy sensitivity shows the clear $1/f$ character of the low-frequency noise. The inset shows the biasing scheme of the feedback loop. The gate was modulated with a square wave at a frequency of 100 Hz and an amplitude of about half of the gate periodicity $\Delta V_g/2$. The output of the SET was synchronously detected with a lock-in amplifier so that the output was only sensitive to dc changes in the gate voltage,

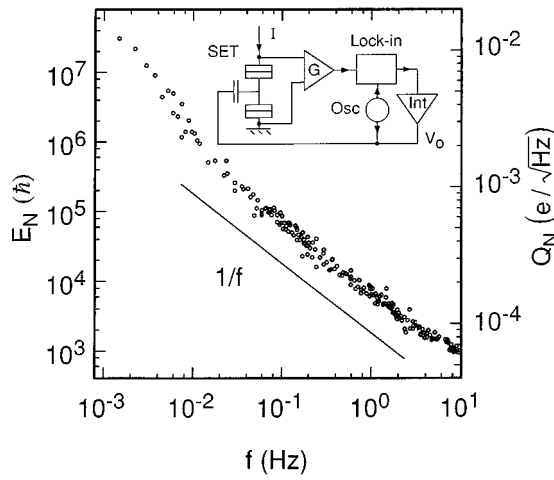


FIG. 3. Energy sensitivity of the SET transistor as a function of frequency. The axis on the right hand side gives the equivalent charge noise. The line indicates the $1/f$ character of the noise. The inset shows the feedback scheme.

measuring directly the input charge noise $Q_N = C_g V_N$. At 10 Hz, the charge noise was $7 \times 10^{-5} e/\sqrt{\text{Hz}}$ corresponding to an energy sensitivity of $1000 \hbar$, which is better than earlier reported values for *planar interdigital* SET transistors.¹⁷ Although the amorphous SiO is known to contain a relatively high density of traps and defects which one would expect to increase the charge noise of the device, the noise is *not* increased by the use of evaporated SiO as a dielectric. The Al-AlO_x-SiO-Al SET transistor was biased in the gain region and an input charge noise Q_N of $4 \times 10^{-4} e/\sqrt{\text{Hz}}$ was measured. This is an order of magnitude reduction of the noise compared to previous experimental results using *overlap* SET transistors with voltage gain.¹⁰

An important reason for using overlap capacitors is the possibility to reduce cross capacitances. The cross capacitance was derived from $I-V_g$ curves of a four junction series array with overlap gates, similar to the one shown in Fig. 1(b). The middle gate polarizes the middle island but also influences the neighboring island via an unwanted cross capacitance. The outer gates are tuned such that the Coulomb blockade of the device is maximized. Then the middle gate is swept recording the $I-V_g$ trace. We have compared traces of an earlier planar design with the overlap design. From Fourier analysis of the $I-V_g$ trace of the overlap array, a gate capacitance of 0.10 fF and a cross capacitance of 8 aF is obtained. This results in a cross talk of only 8%. In compari-

son, the cross capacitances with coplanar gates are typically 40%. The reduced cross talk to the neighboring island due to use of overlap capacitors allows the use of Fourier analysis as a versatile tool for obtaining the capacitances in more complex SET circuits. Optimization procedures for canceling the cross talk by tuning the gates individually⁵ can thus be avoided.

In summary, we have developed a multilayer fabrication process for SET devices. We have used this process to integrate submicron overlap capacitors with SET devices. These devices exhibit voltage gain, low cross capacitance and an order of magnitude improvement in the charge noise compared to the SET transistors with overlap capacitors fabricated previously. Moreover, this process allows for the fabrication of tunnel junctions at different levels, opening the possibility of integrating SET devices in different layers of the circuitry.

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¹ T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. **59**, 109 (1987).

² K. K. Likharev, IEEE Trans. Magn. **23**, 1142 (1987).

³ T. A. Fulton, P. L. Gammel, and L. N. Dunkleberger, Phys. Rev. Lett. **67**, 3148 (1991).

⁴ P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, and M. H. Devoret, Z. Phys. B **85**, 327 (1991).

⁵ John M. Martinis and M. Nahum, Phys. Rev. Lett. **72**, 904 (1994).

⁶ L. J. Geerligs, V. F. Andereg, P. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64**, 2691 (1990).

⁷ H. Pothier, P. Lafarge, P. F. Orfila, C. Urbina, D. Esteve, and M. H. Devoret, Physica B **169**, 573 (1991).

⁸ See for reviews D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomenon in Solids*, edited by B. L. Altshuler, P. A. Lee, and R. A. Webb; *Single Charge Tunneling, Coulomb Blockade Phenomena in Nanostructures*, edited by M. H. Devoret and H. Grabert, NATO ASI Series B: Physics 294 (Plenum, New York, 1991).

⁹ G. J. Dolan, Appl. Phys. Lett. **31**, 337 (1977).

¹⁰ G. Zimmerli, R. L. Kautz, and John M. Martinis, Appl. Phys. Lett. **61**, 2616 (1992).

¹¹ D. B. Haviland, L. S. Kuzmin, P. Delsing, K. K. Likharev, and T. Claeson, Z. Phys. B **85**, 339 (1991).

¹² K. K. Likharev, IBM J. Res. Dev. **31**, 144 (1988).

¹³ D. V. Averin and Yu. V. Nazarov, Phys. Rev. Lett. **65**, 2446 (1990).

¹⁴ J. M. Martinis, M. H. Devoret, and J. Clarke, Phys. Rev. B **35**, 4682 (1987).

¹⁵ A. N. Korotkov, D. V. Averin, K. K. Likharev, and S. A. Vasenko, in *Single Electron Tunneling and Mesoscopic Devices*, edited by H. Koch (Springer, New York, 1992), p. 45.

¹⁶ J. Clarke, W. M. Goubau, and M. B. Ketchen, J. Low Temp. Phys. **25**, 99 (1976).

¹⁷ See for example, L. S. Kuzmin, P. Delsing, T. Claeson, and K. K. Likharev, Phys. Rev. Lett. **62**, 2539 (1989); L. J. Geerligs, V. F. Andereg, and J. E. Mooij, Physica B **165**, 937 (1990).