



<https://commons.wikimedia.org/wiki/File:Transistors.agr.jpg>



https://www.k-ai.at/wp-content/uploads/2023/11/K-AI_imagebilder_30082023_519.jpg

Physics of semiconductor devices

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October 7, 2026

Physics of semiconductor devices

- Diodes, solid state lasers, transistors
- Computing, communications
- Controllers: vacuum cleaners, coffee makers, etc.
- Transportation, autonomous driving, electric cars
- Efficient lighting, solar cells, displays
- Lasers



PHT.301 Physics of Semiconductor Devices

Outline

Home
Outline
Introduction
Electrons in crystals
Intrinsic Semiconductors
Extrinsic Semiconductors
Transport
pn junctions
Contacts
JFETs/MESFETs
MOSFETs
Bipolar transistors
Opto-electronics
Lectures
Books
Exam questions
Mathematical expressions
TUG students
Student projects

• **Introduction**

- Semiconductors, transistors, and the electronics industry

• **Semiconductor crystals**

- Energy bands **W**
 - Crystal structure **W**
 - Bravais lattice **W**
 - Miller indices **W**
 - Examples of crystal structures **W**
 - silicon, GaN (wurzite), SiC 4H, ZnO (wurzite), diamond
 - simple cubic, fcc, bcc, hcp, zincblende
 - Wave and particle nature of electrons
 - k-space
 - Density of states **W** Some examples: Al fcc, Au fcc, Cu fcc, Pt fcc, W bcc, Si diamond, Gra
 - Pauli exclusion principle **W**
 - Fermi function **W**
 - Fermi energy **W**
 - Metals, semiconductors, and insulators
 - Metal band structure
 - Semiconductor band structure
- Absorption and emission of photons
- Direct and indirect band gaps **W**

• **Intrinsic semiconductors**

- Conduction band
- Valence band
- Effective mass **W**
- Holes **W**
- Boltzmann approximation
- Law of mass action **W**
- Fermi energy of an intrinsic semiconductor **EN 2:36**
- Intrinsic semiconductors with a split-off band

Examination

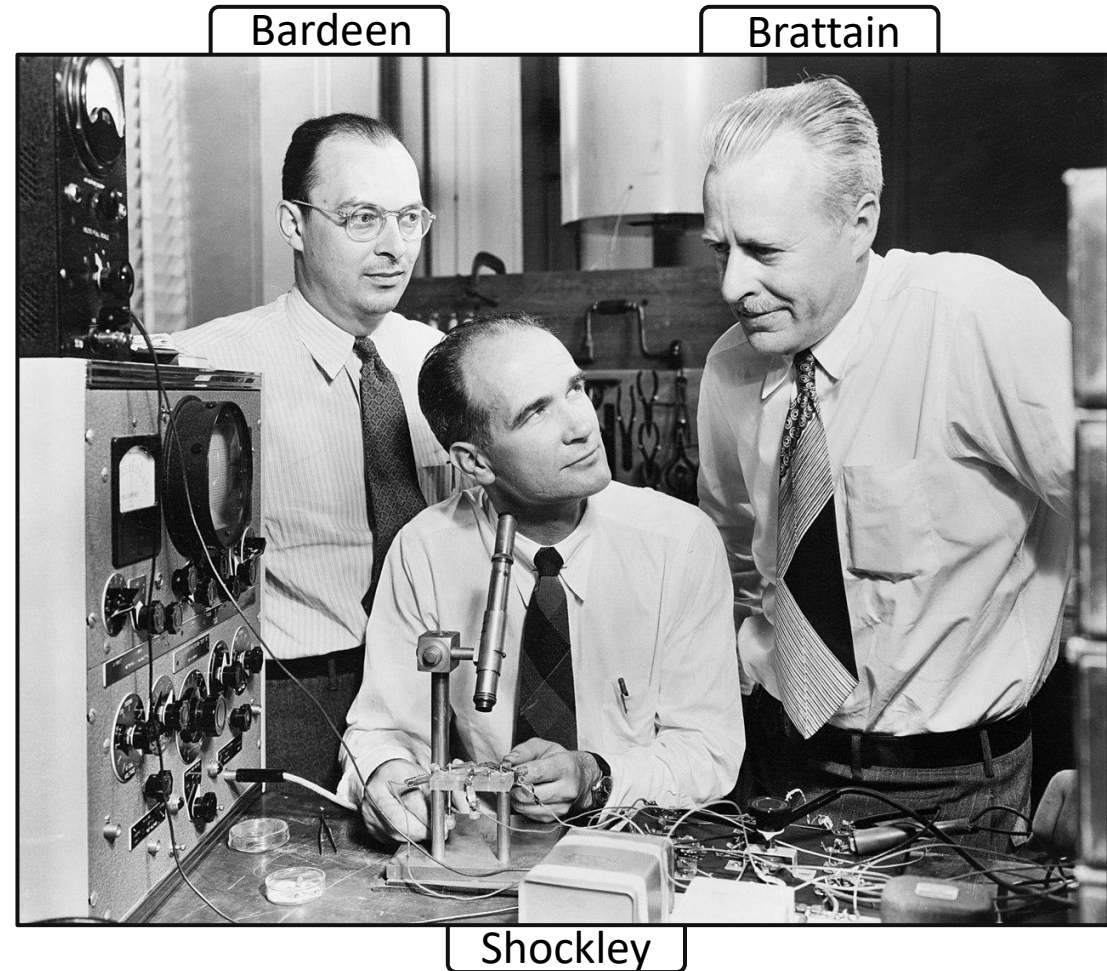
1 hour written exam

one page of handwritten notes

Oral exam

The first point contact transistor

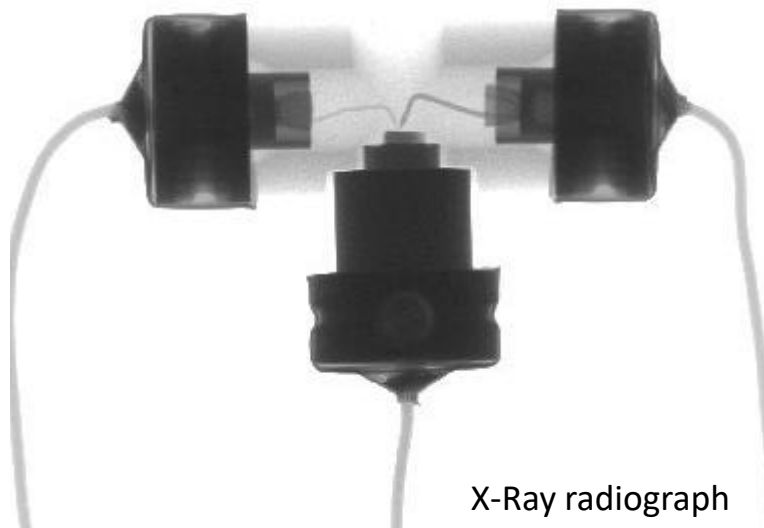
William Shockley, John Bardeen, and Walter Brattain
Bell Laboratories, Murray Hill, New Jersey (1947)



https://upload.wikimedia.org/wikipedia/commons/thumb/c/c2/Bardeen_Shockley_Brattain_1948.JPG/1280px-Bardeen_Shockley_Brattain_1948.JPG

The “second” point contact transistor: TRANSISTRON

CFS Westinghouse, Subsidiary Paris (1948)

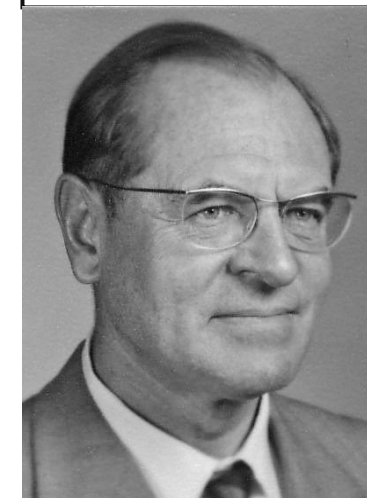


X-Ray radiograph

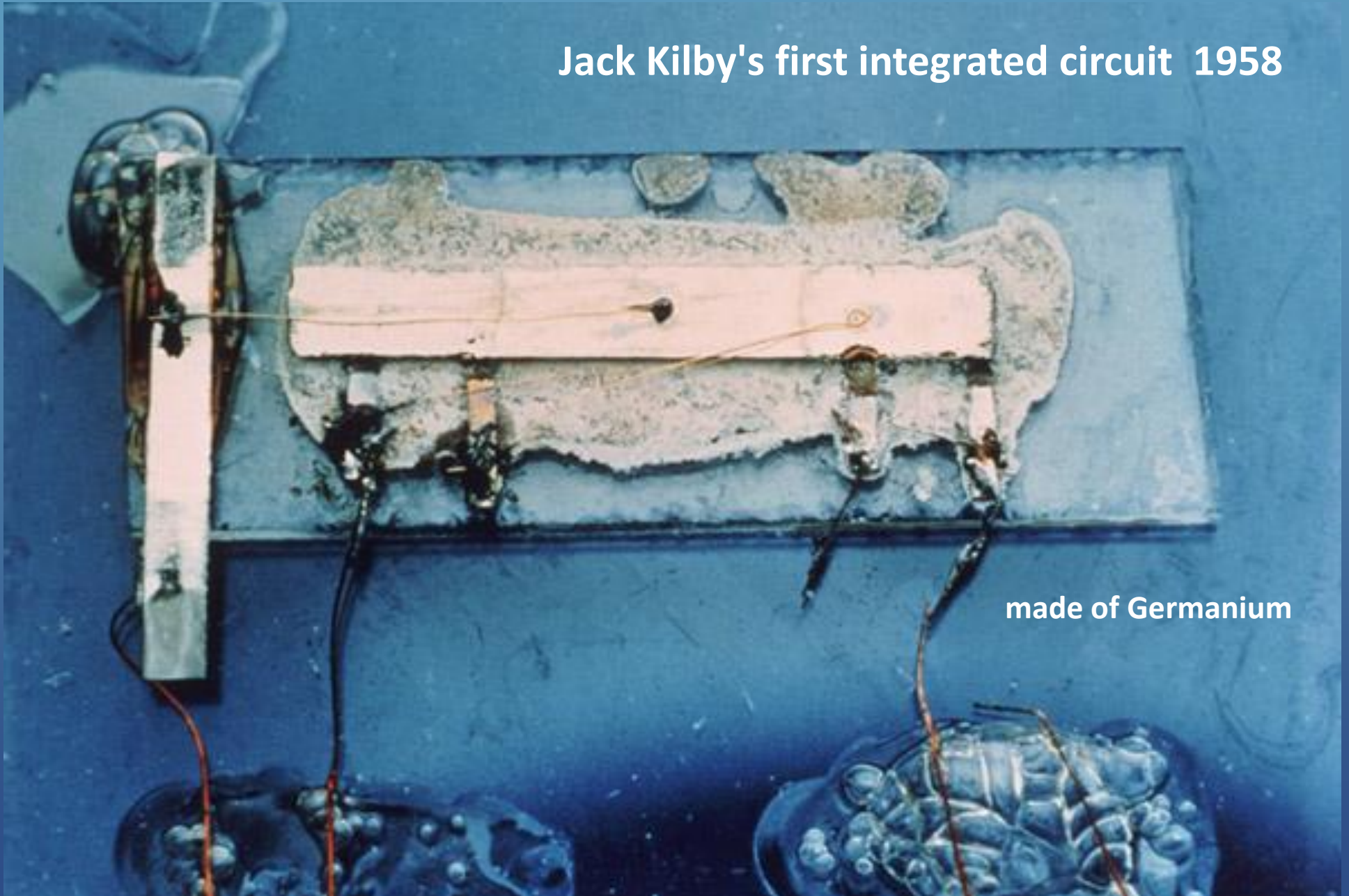
Heinrich Welker



Herbert Mataré

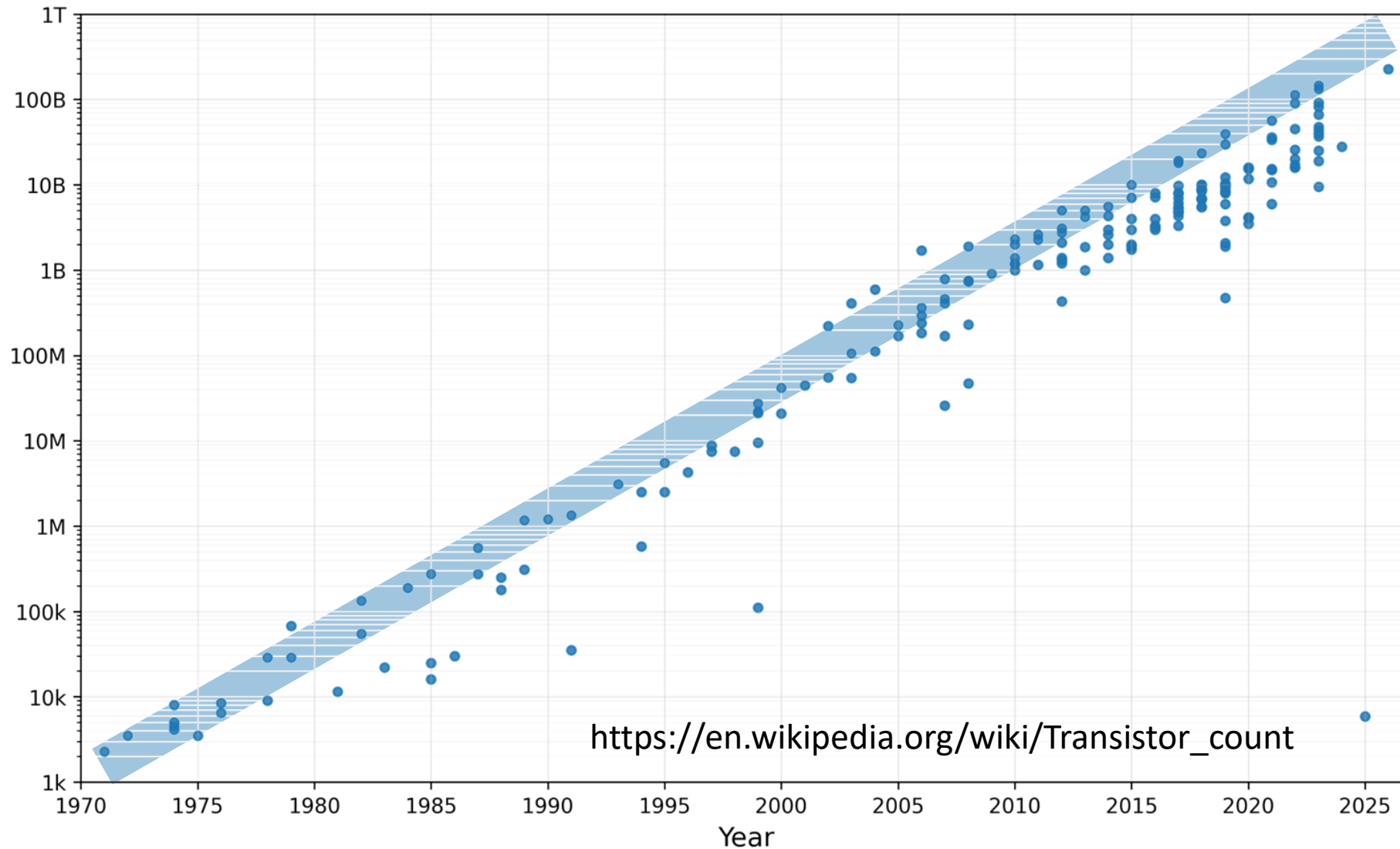


Jack Kilby's first integrated circuit 1958



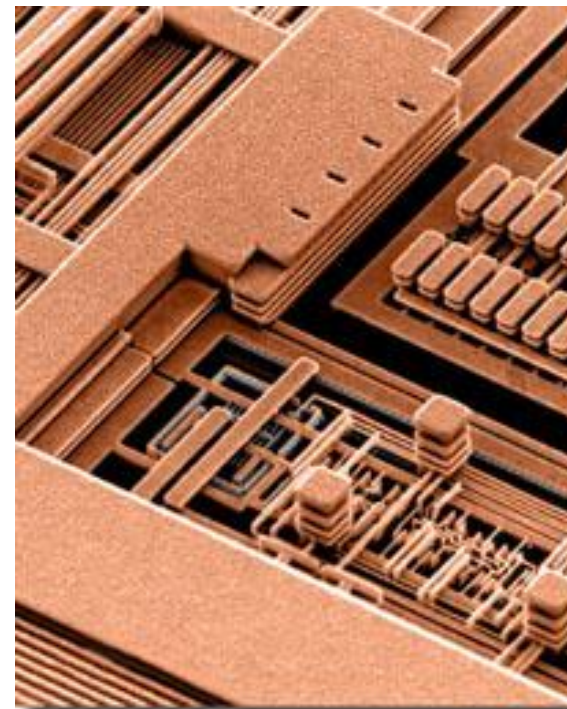
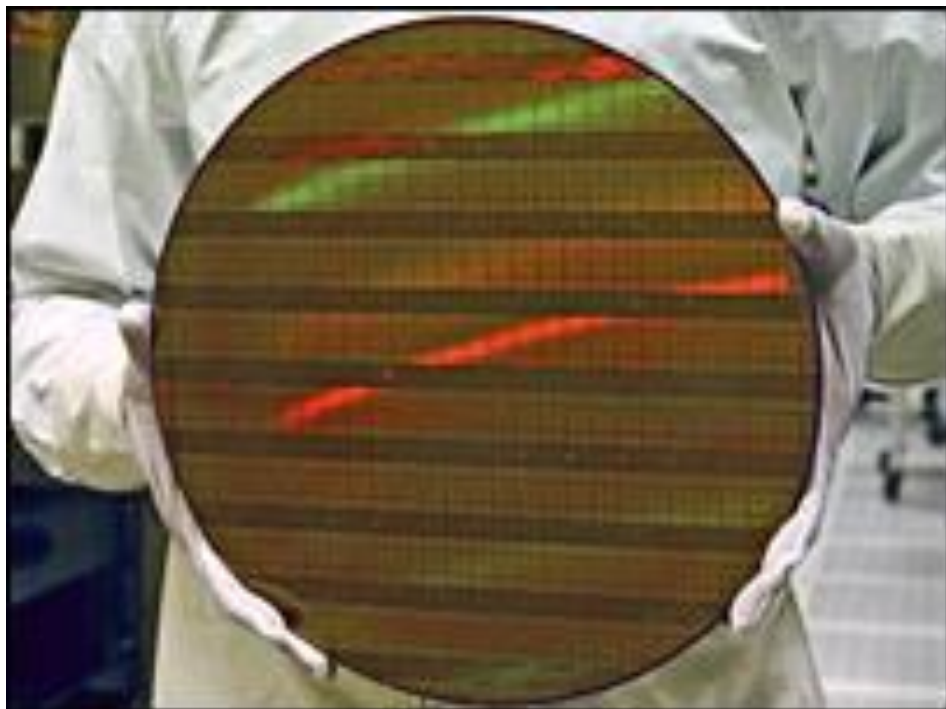
made of Germanium

The number of transistors double every two years.



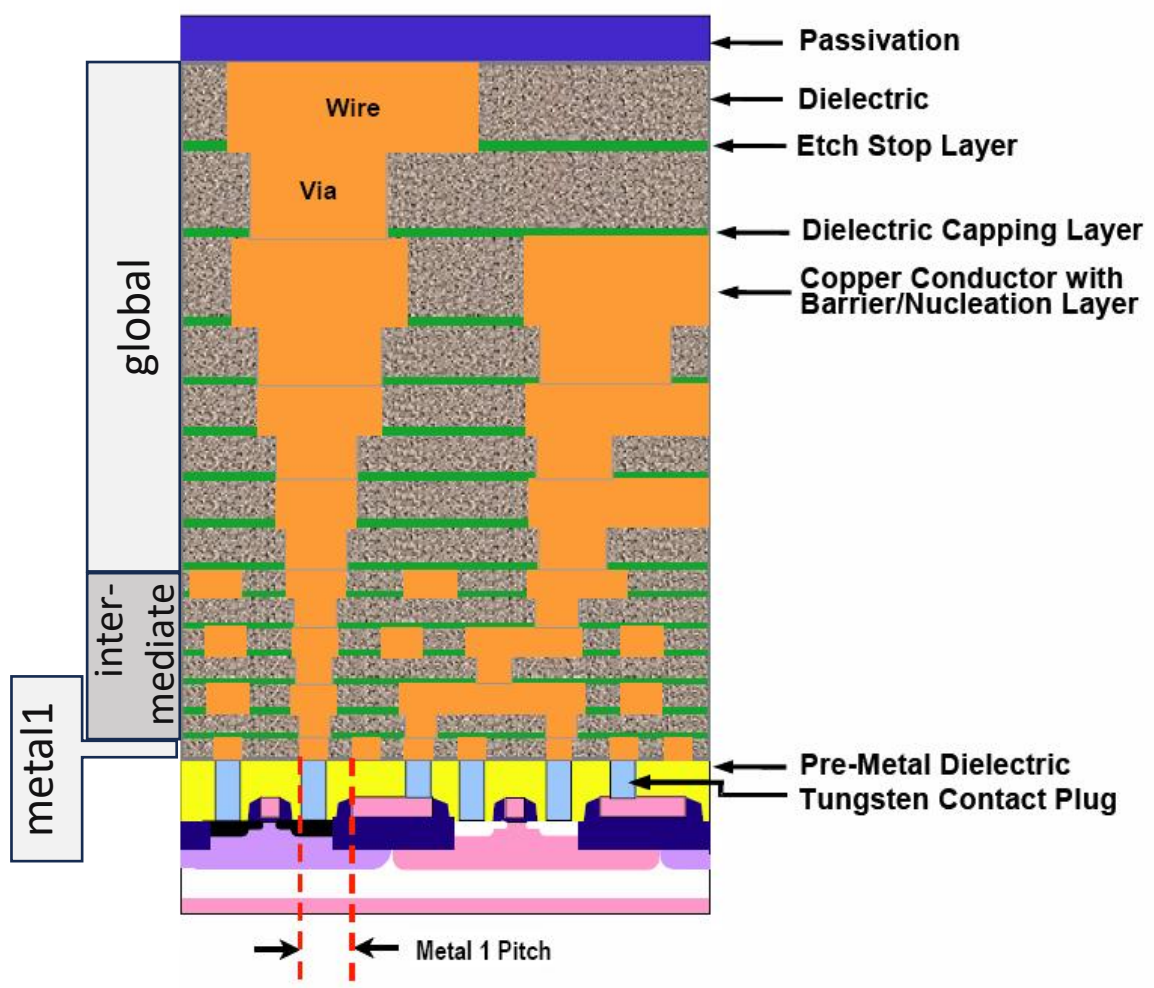
https://en.wikipedia.org/wiki/Transistor_count

3-atom-thick MoS₂
on sapphire



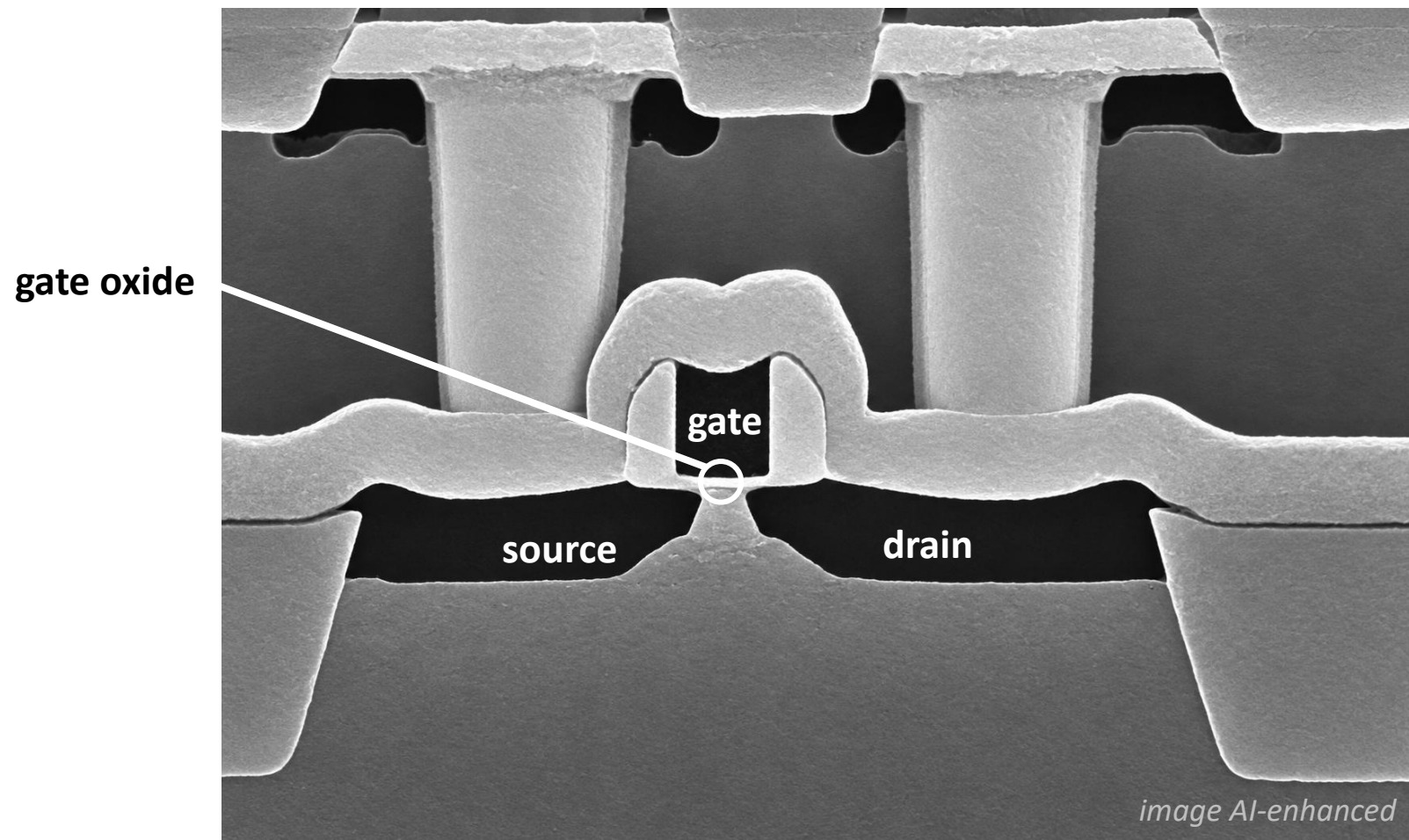
PIDS2a

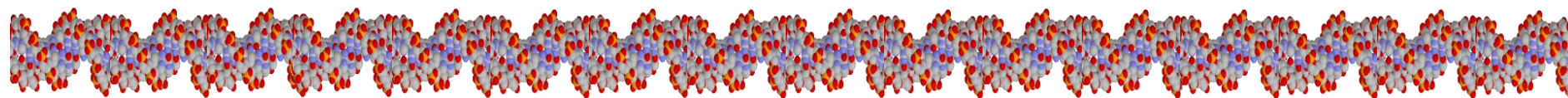
High-Performance (HP) Logic Technology Requirements



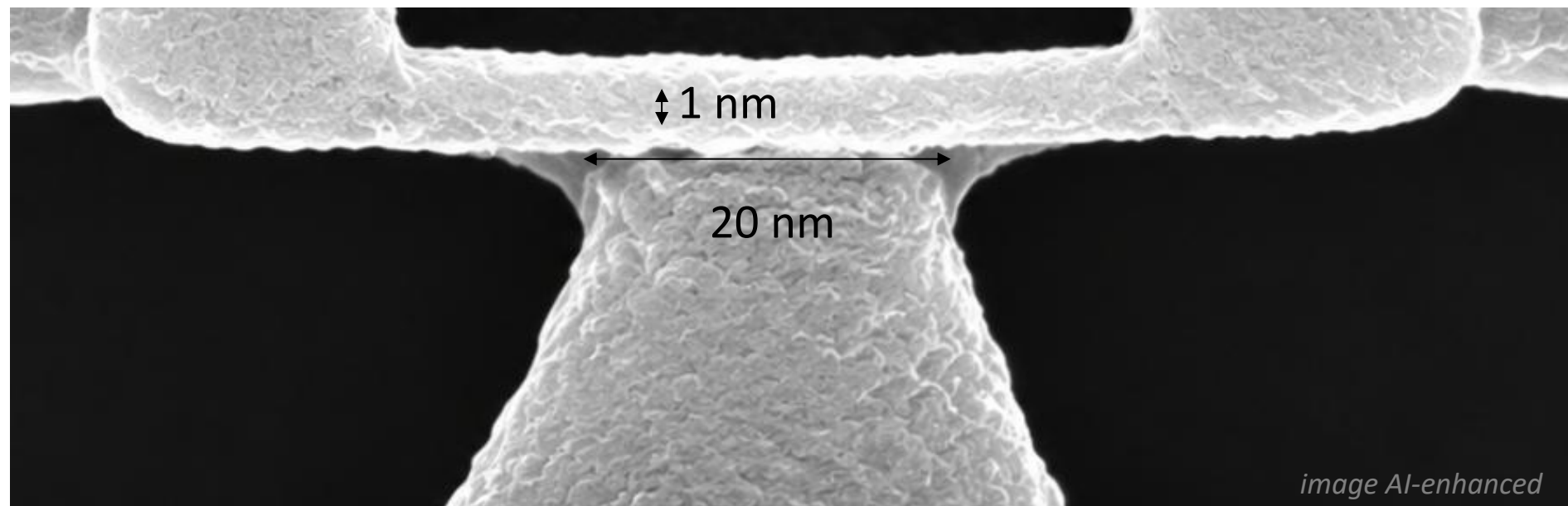
year	metal 1/2 pitch	gate length
2013	20	16.0
2014	18	14.4
2015	16.7	13.4
2016	15.2	12.2
2017	13.9	11.1
2018	12.7	10.2
2019	11.6	9.3
2020	10.6	8.5
2021	9.7	7.8
2022	8.8	7.0
2023	8.0	6.4
2024	7.3	5.8
2025	6.7	5.4
2026	6.1	4.9
2027	5.6	4.5
2028	5.1	4.1

in nanometers



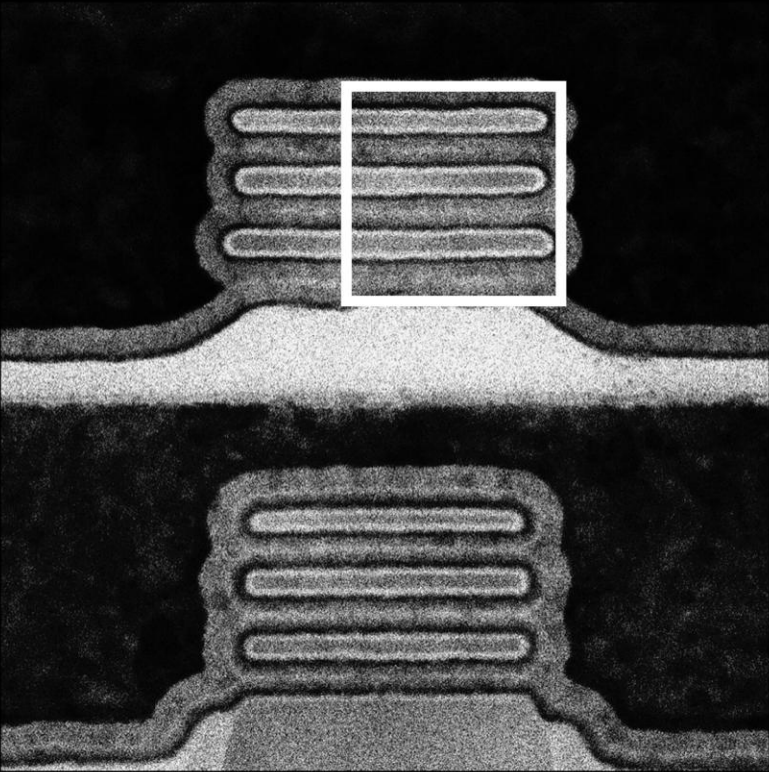


DNA

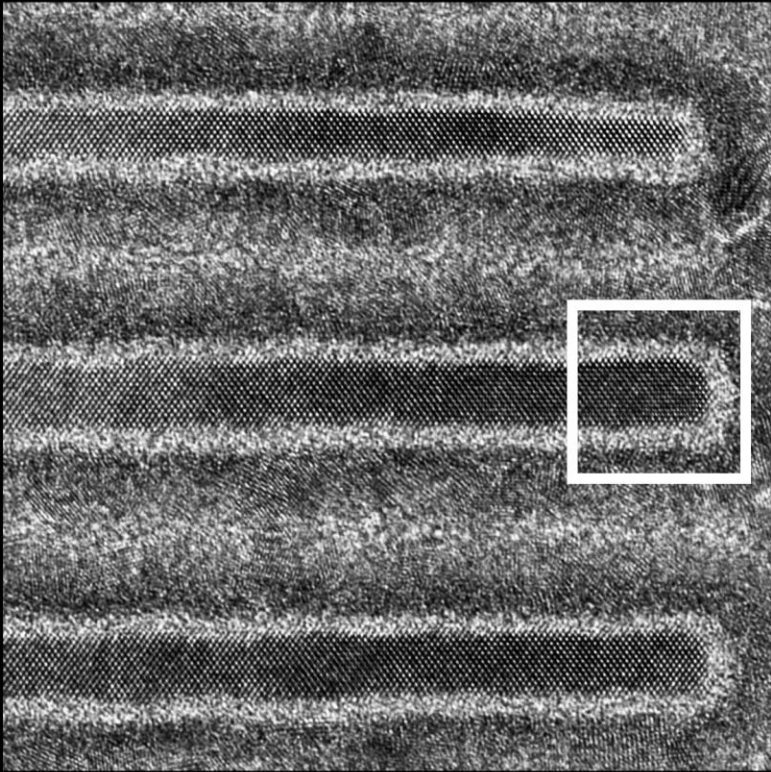


MOSFET

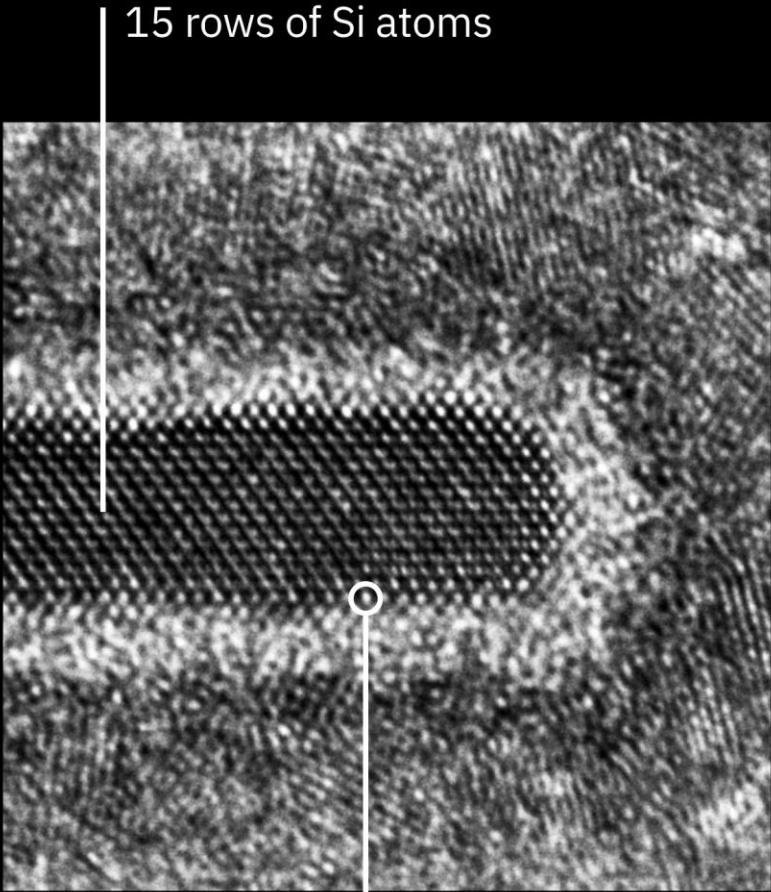
Sub-1nm
Chip Technology



20nm



10nm



4.5nm

Silicon (Si) atom



research.ibm.com

<https://newsroom.ibm.com/2026-06-25-ibm-debuts-worlds-first-sub-1-nanometer-chip-technology>



<https://irds.ieee.org>

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™



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ROADMAP
FOR
DEVICES AND SYSTEMS

2017 EDITION

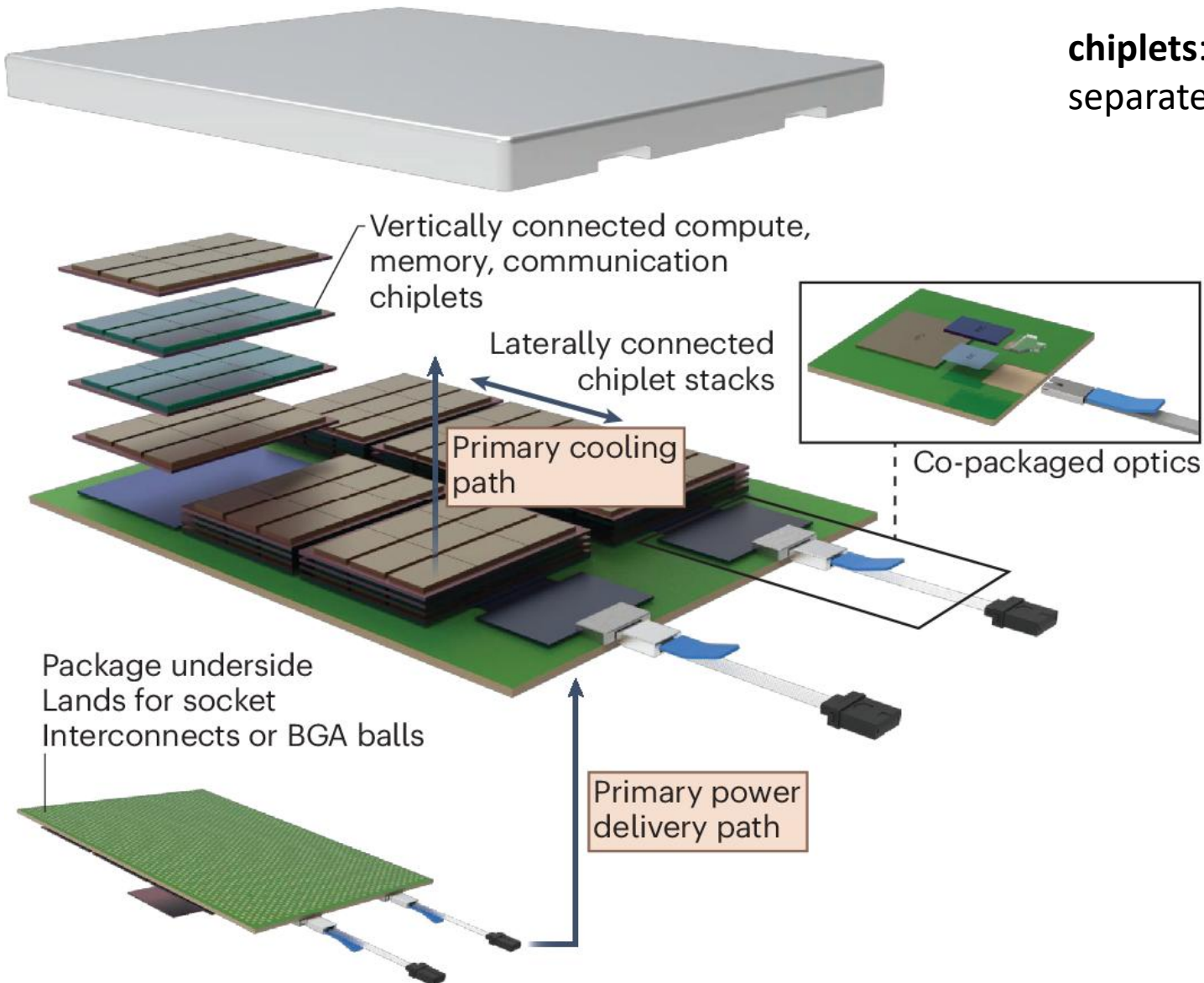
EXECUTIVE SUMMARY

1. Application Benchmarking (AB)
2. Systems and Architectures (SA)
3. Outside System Connectivity (OSC)
4. More Moore (MM) ←
5. Beyond CMOS (BC) ←
6. Packaging Integration (PI)
7. Factory Integration (FI)
8. Lithography (L)
9. Emerging Research Materials (ERM) ←
10. Yield Enhancement (YE)
11. Metrology (M)
12. Environment, Safety, Health (ESH/S), and Sustainability

Advanced packaging of chiplets for future computing needs

chiplets:

separate functional blocks like logic, memory, and I/O

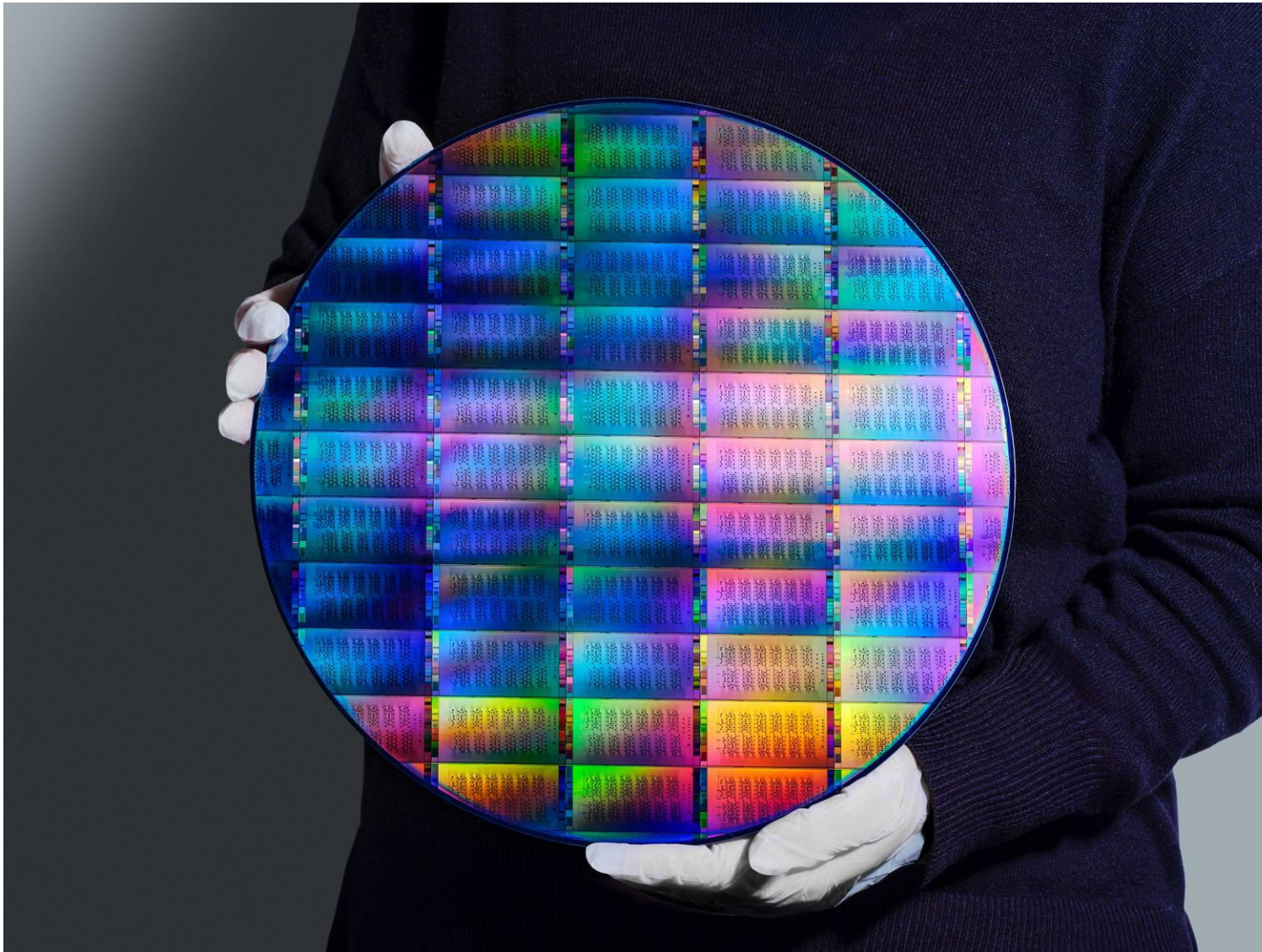


different blocks can use optimized manufacturing process nodes

blocks can differ in semiconducting material

required:

interconnects (high speed, low latency)



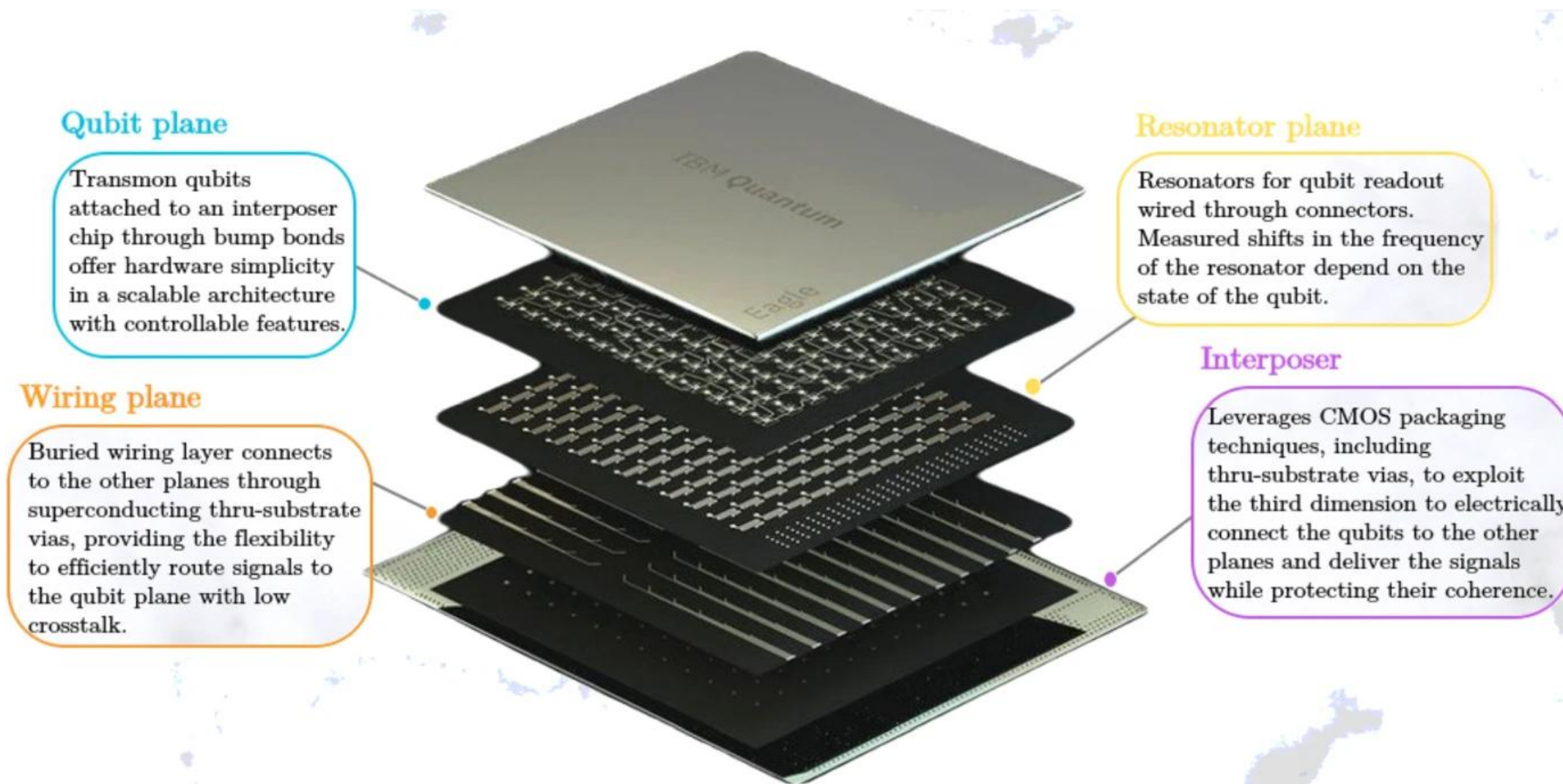
300mm IBM Quantum Nighthawk
wafer (Credit: IBM)

<https://www.ibm.com/quantum/blog/300mm-fab>

from a semiconductor device fab

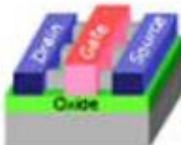
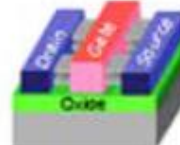
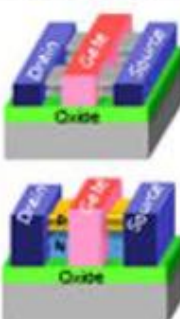
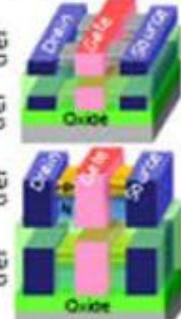
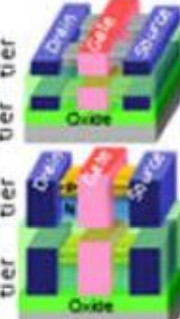
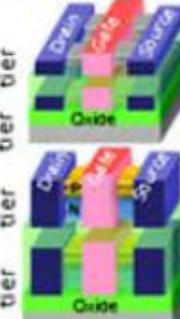
**limit of on-chip scaling:
qubit cross-talk**

Modularity also key for quantum computing





INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16 T2	G38M16 T4	G38M16 T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN separation width (nm)	45	40	20	15	15	10

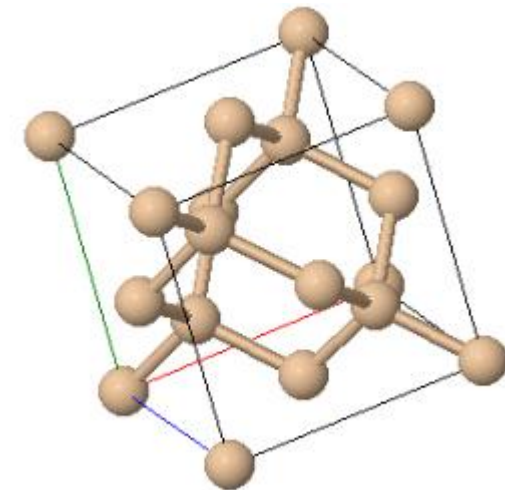
Si: $\sigma = 4.3 \times 10^{-4} \text{ 1}/\Omega \cdot \text{m}$

[illegible]

Silicon

- important semiconducting material
- 2nd most common element on earth's crust (rocks, sand, glass, concrete)
- often doped with other elements
- oxide SiO_2 is a good insulator

2.33		28.086
	Si	
5.43		14
	$3s^2 3p^2$	
1683	DIA	625



silicon crystal = diamond crystal structure

Wolfgang Pauli has lost his interest in Solid State Physics ...

in a letter to his assistant **Rudolf Peierls** (Sept. 29, **1931**):

„über Halbleiter soll man nicht arbeiten, das ist eine Schweinerei,
wer weiß ob es überhaupt Halbleiter gibt.“

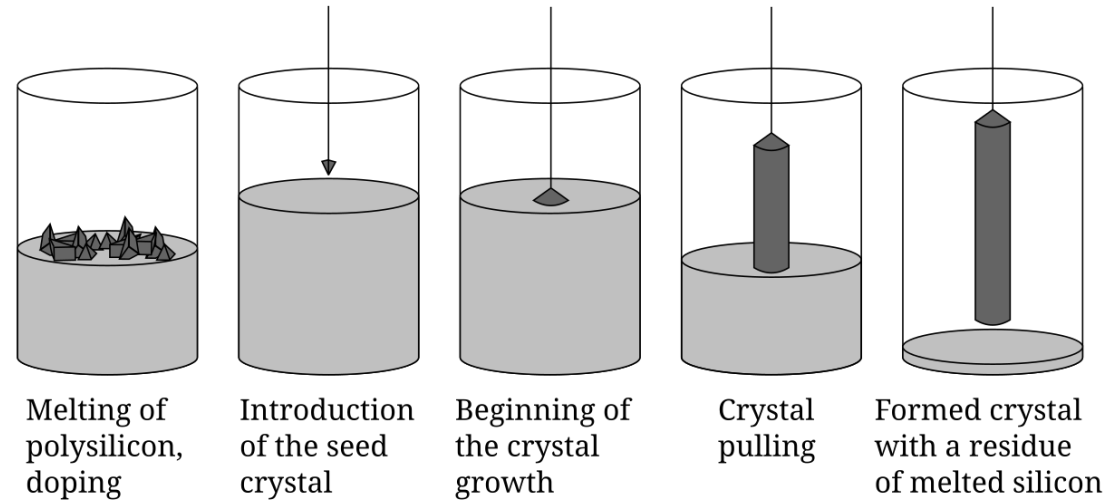
*“You shouldn't work on semiconductors, it's a mess, who knows if
semiconductors even exist.”*

Silicon

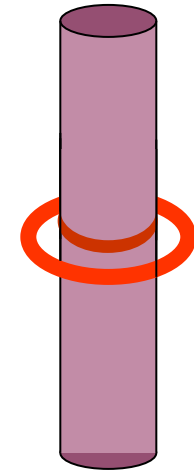
Large (2 m) single crystals are grown



Czochralski process

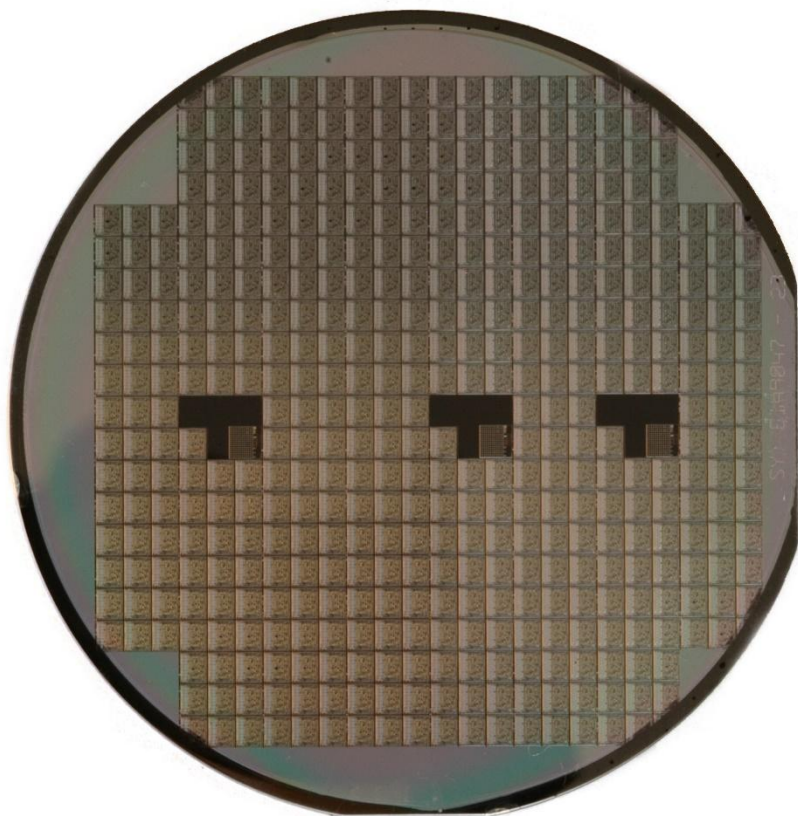


Float zone



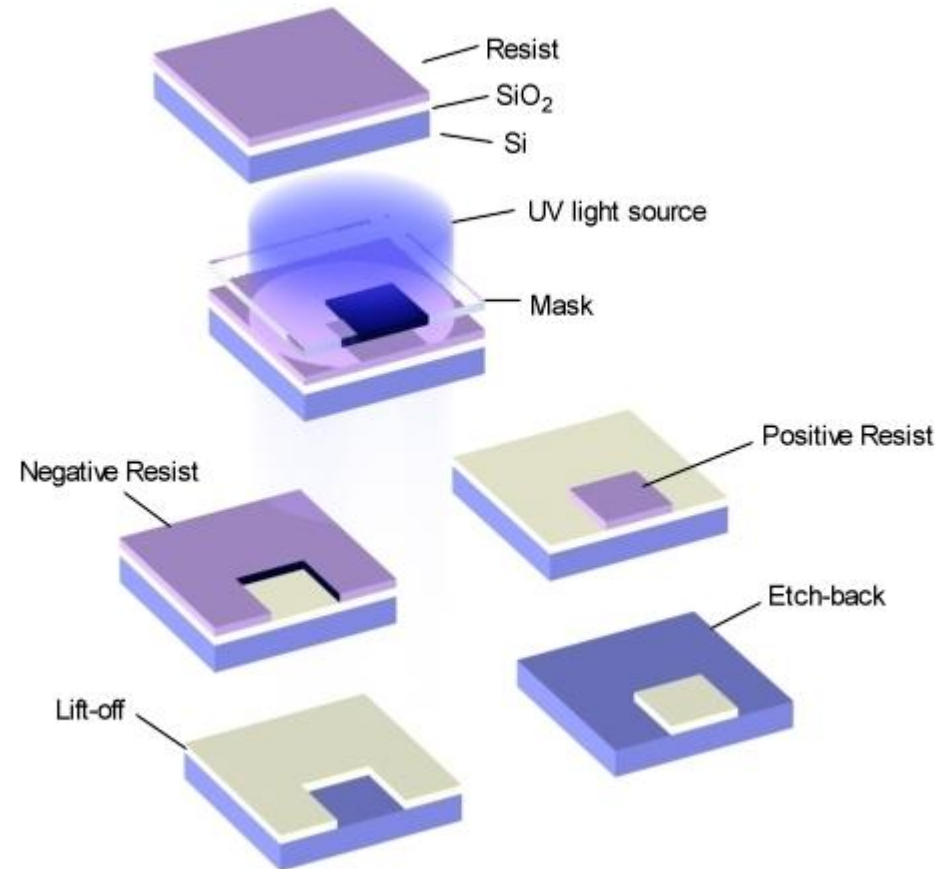
http://en.wikipedia.org/wiki/Czochralski_process

Silicon wafers



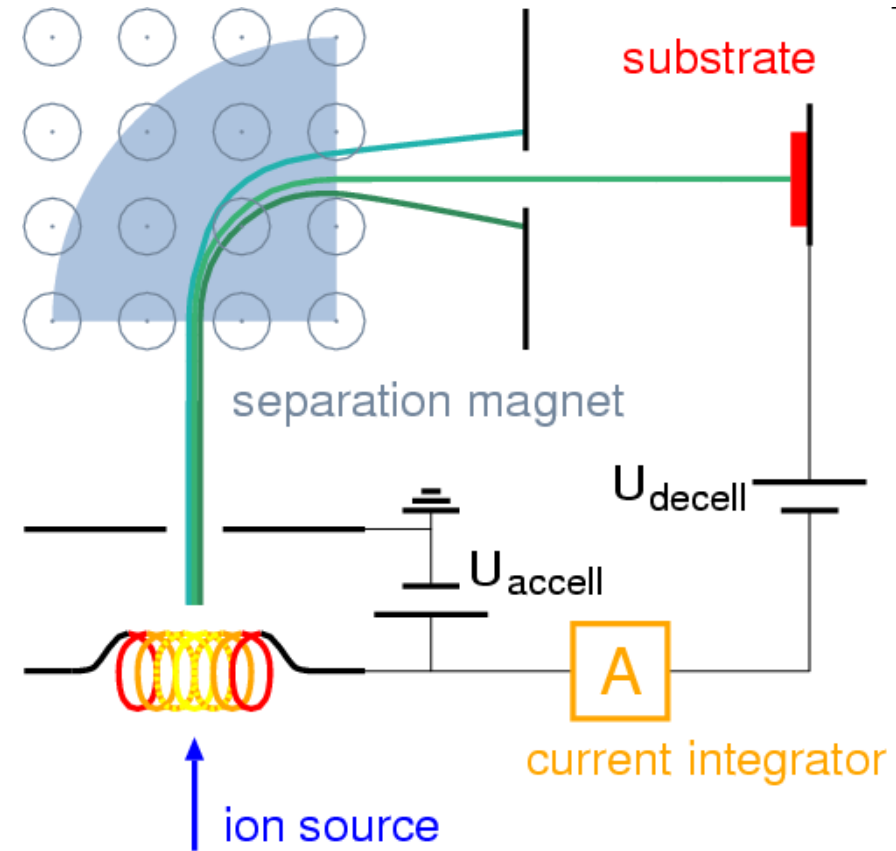
50 mm - 0.5 mm thick

Photolithography



<http://britneyspears.ac/physics/fabrication/photolithography.htm>
<http://cleanroom.byu.edu/lithography.parts/Lithography.html>

Ion implantation



Implant at 7° to avoid channeling

On the chip

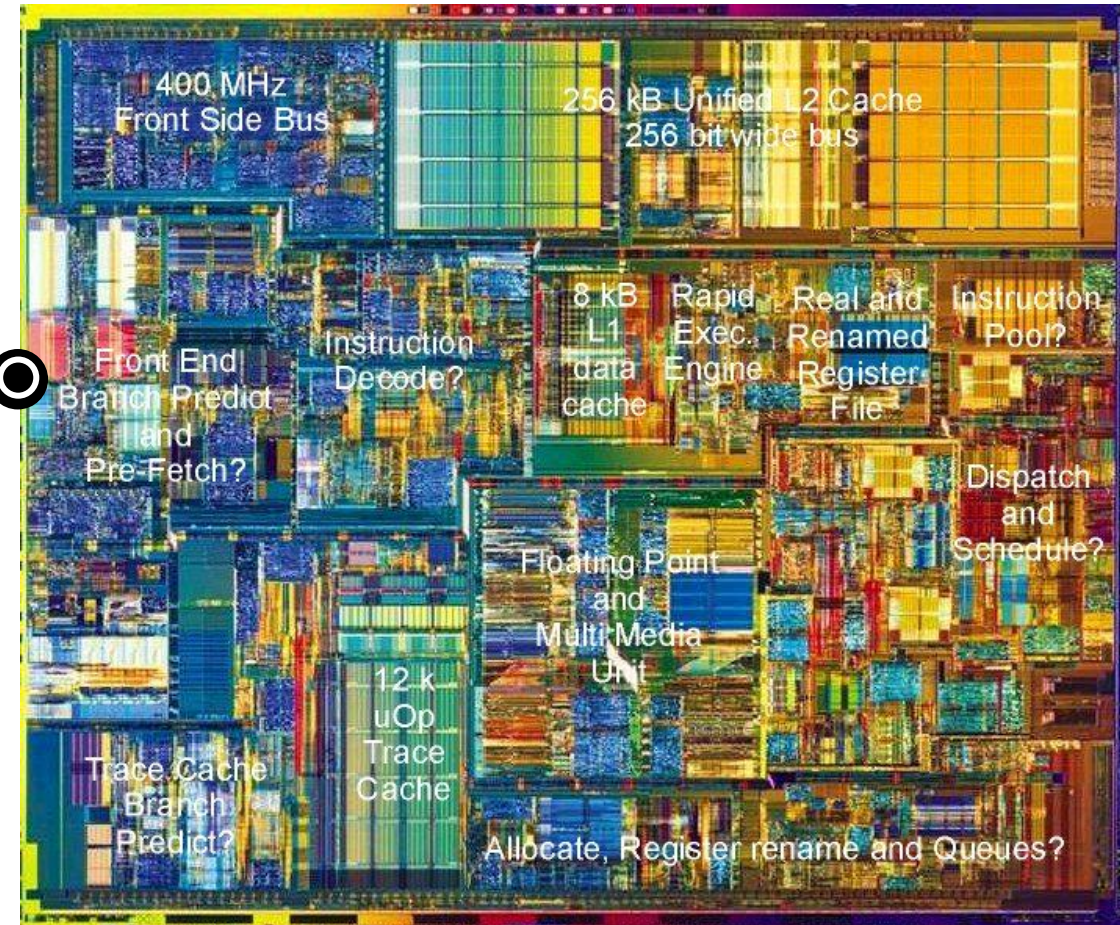
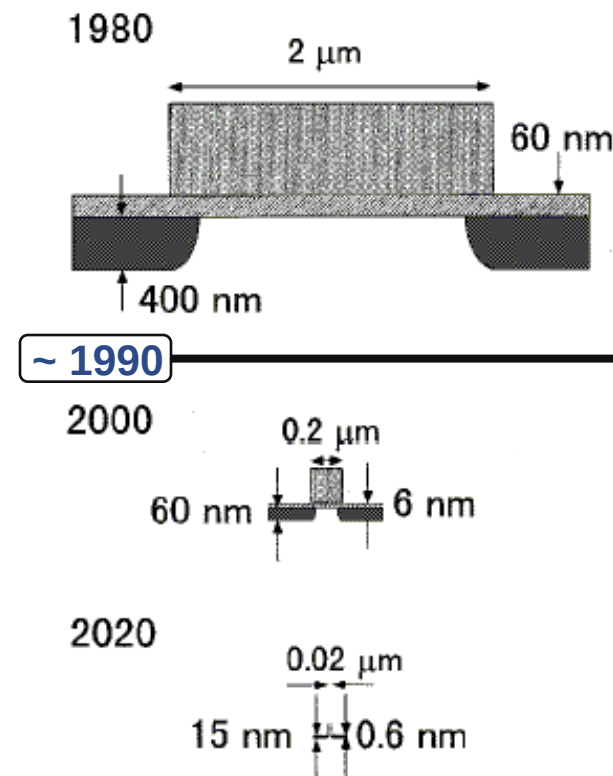
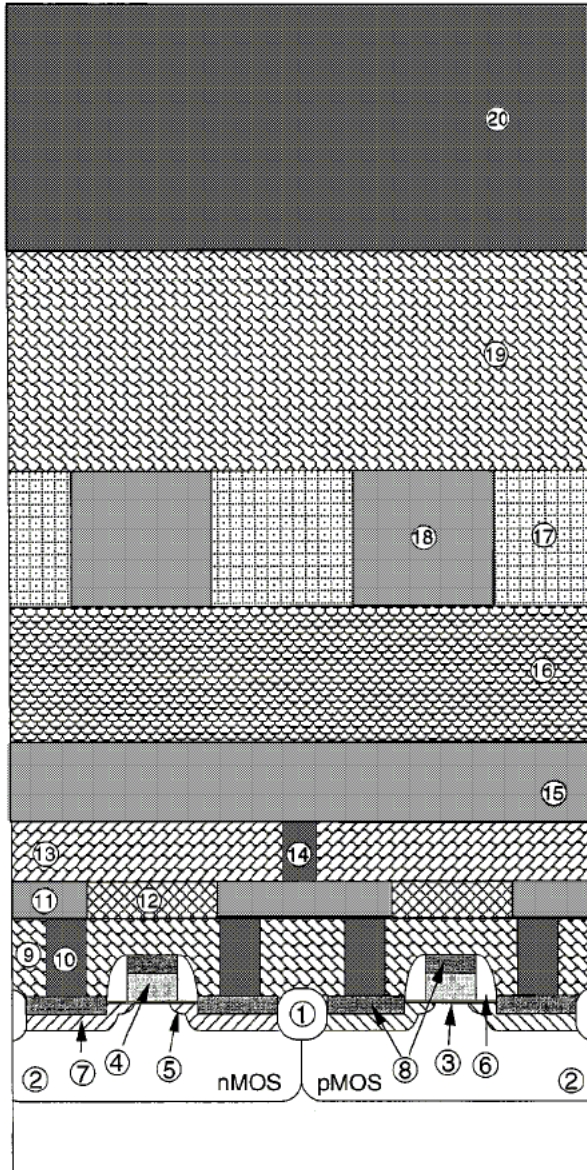


Fig. 2 Schematic cross section of present CMOS FETs with multilayered wiring.