Doping and Oxidation

Franssila: Chapters 13,14, 15

Peter Hadley

Doping

Add donors (n-type) or acceptors (p-type)

10^{12} cm^{-3} impurity limit

10^{21} cm^{-3} solubility limit

Dopants added

during crystal growth (whole wafer)

neutron transmutation (whole wafer)
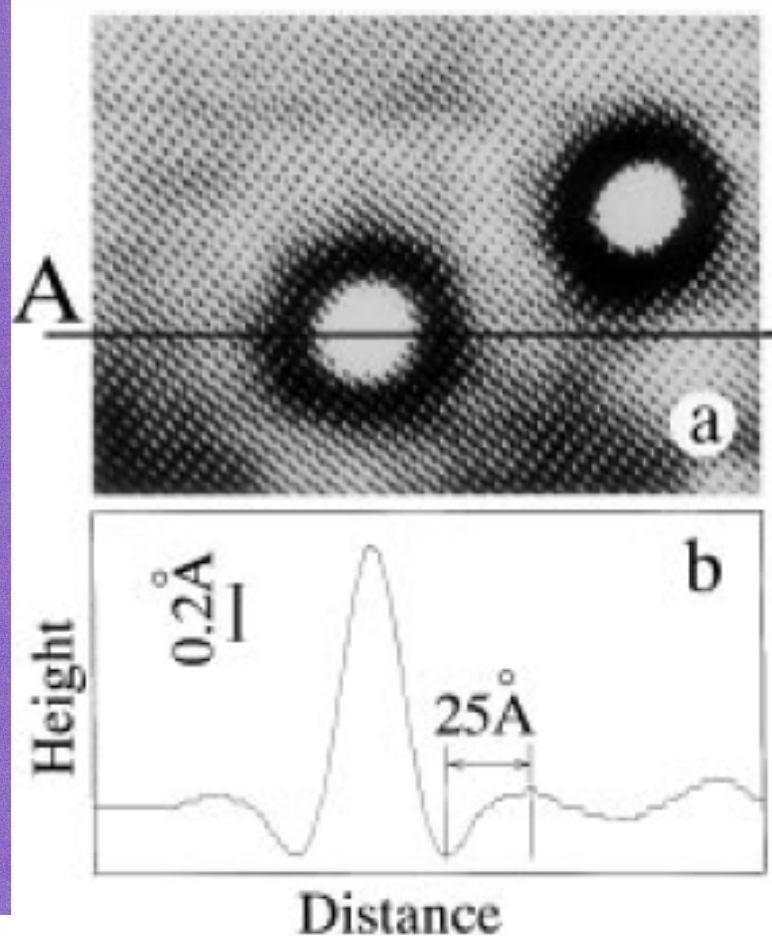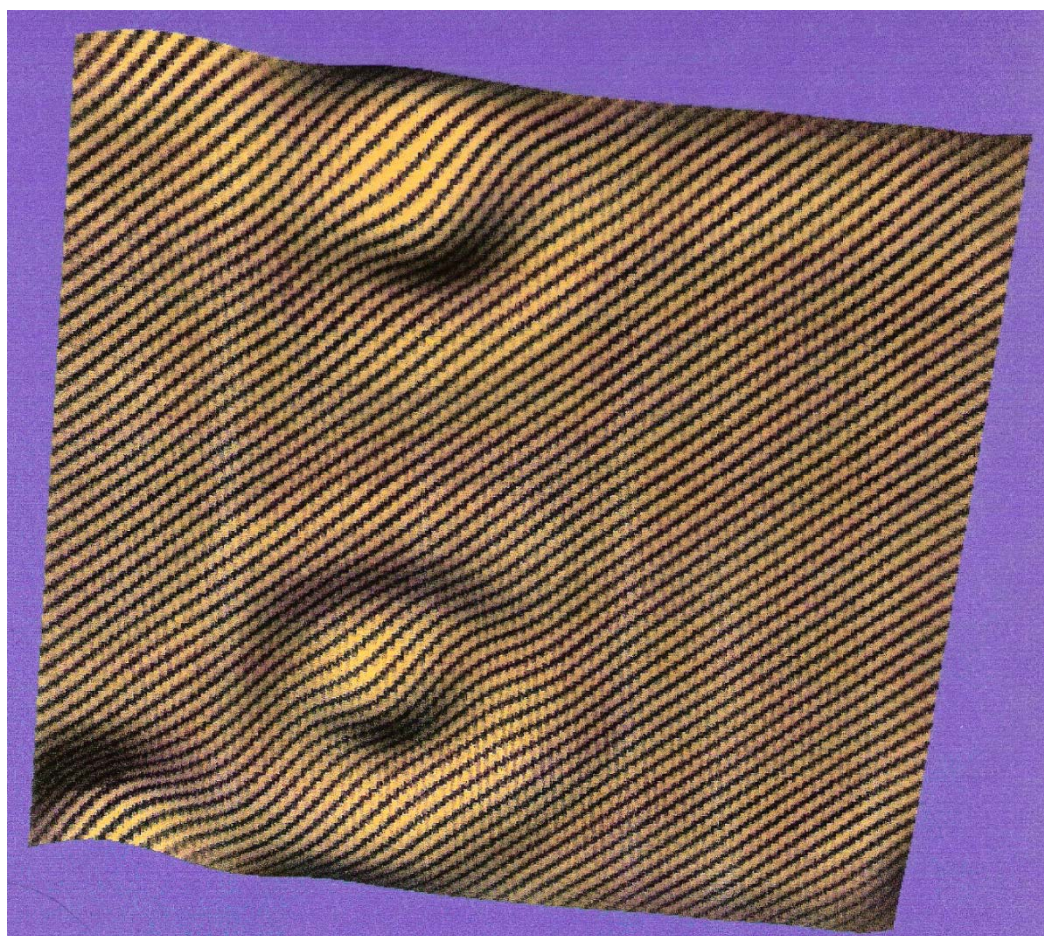
during epitaxy (layers)

diffusion (local)

ion implantation (local)

Direct Observation of Friedel Oscillations around Incorporated Si_{Ga} Dopants in GaAs by Low-Temperature Scanning Tunneling Microscopy

M. C. M. M. van der Wielen, A. J. A. van Roij, and H. van Kempen

Research Institute for Materials, University of Nijmegen, Toernooiveld 1, 6525 ED Nijmegen, The Netherlands
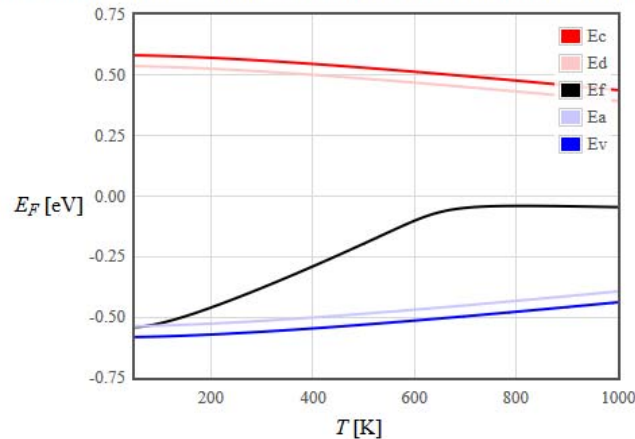(Received 25 July 1995)
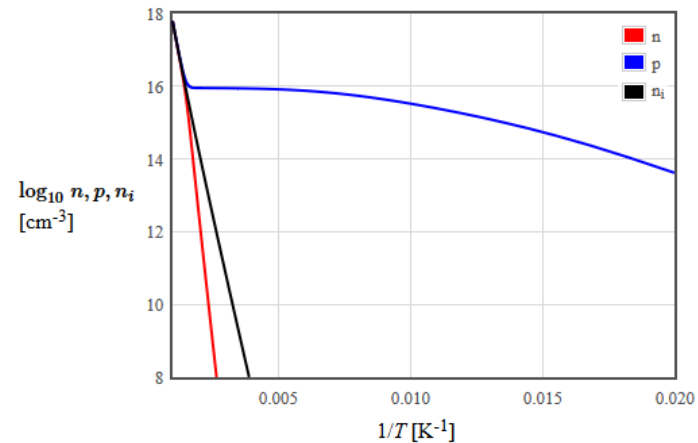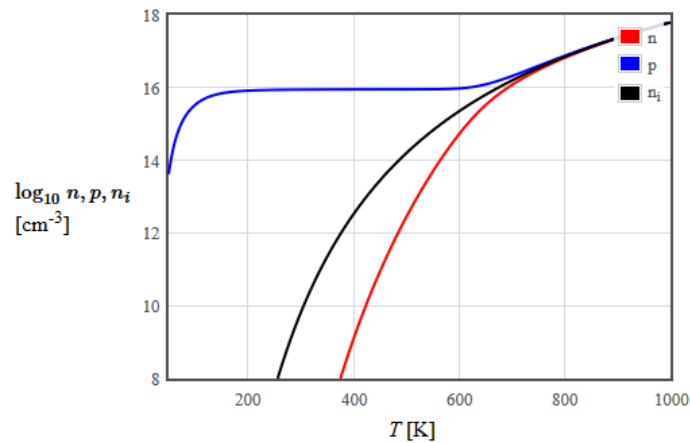
Doping determines the carrier concentration

http://lamp.tu-graz.ac.at/~hadley/psd/L4/eftplot.html

Crystal growth

Czochralski Process
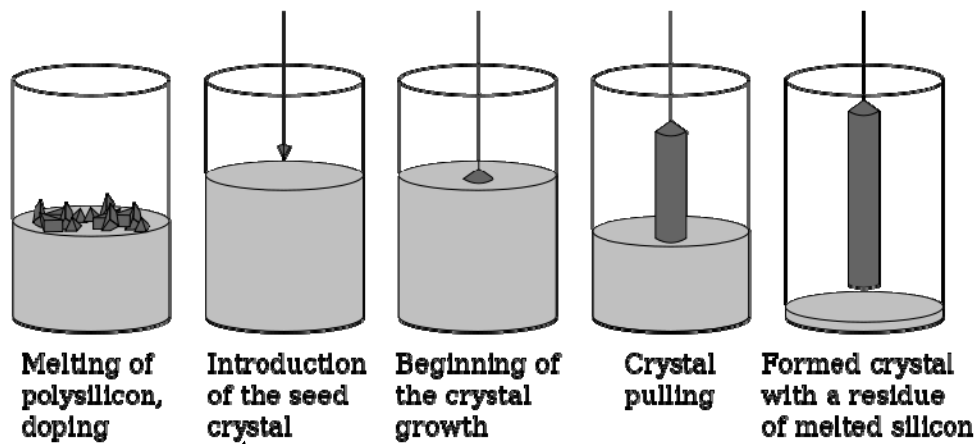
add dopants to the melt

images from wikipedia

Crystal growth

Float zone Process

Neutron transmutation

$$^{30}\text{Si} + \text{n} \rightarrow {}^{31}\text{Si} + \gamma$$
$$^{31}\text{Si} \rightarrow {}^{31}\text{P} + \beta$$
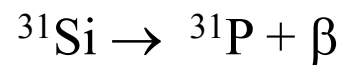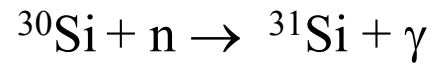
image from wikipedia

Chemical vapor deposition

Source materials + carrier gas

(b): Substrates

(C): heater
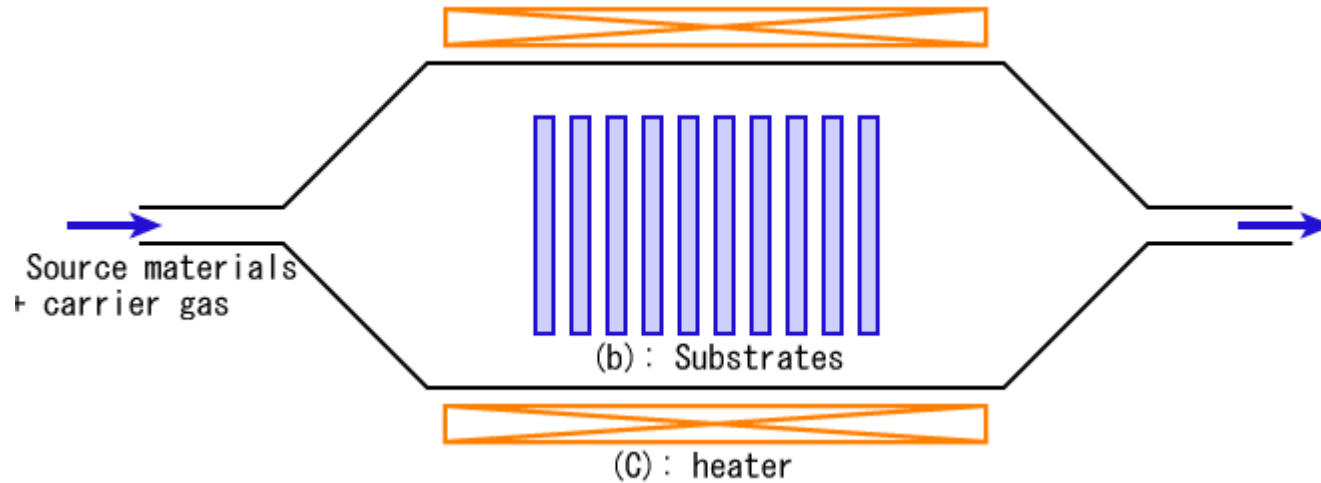
Epitaxial silicon CVD SiH_4 (silane) or SiH_2Cl_2 (dichlorosilane)
PH_3 (phosphine) for n-doping or B_2H_6 (diborane) for p-doping.

The doping can be adjusted in layers.

image from wikipedia

Gas phase diffusion

AsH_3 (Arsine) or PH_3 (phosphine) for n-doping
B_2H_6 (diborane) for p-doping.
100 - 200 wafers in a batch.

Gas phase diffusion

concentration

C_{surf}

x_j depth
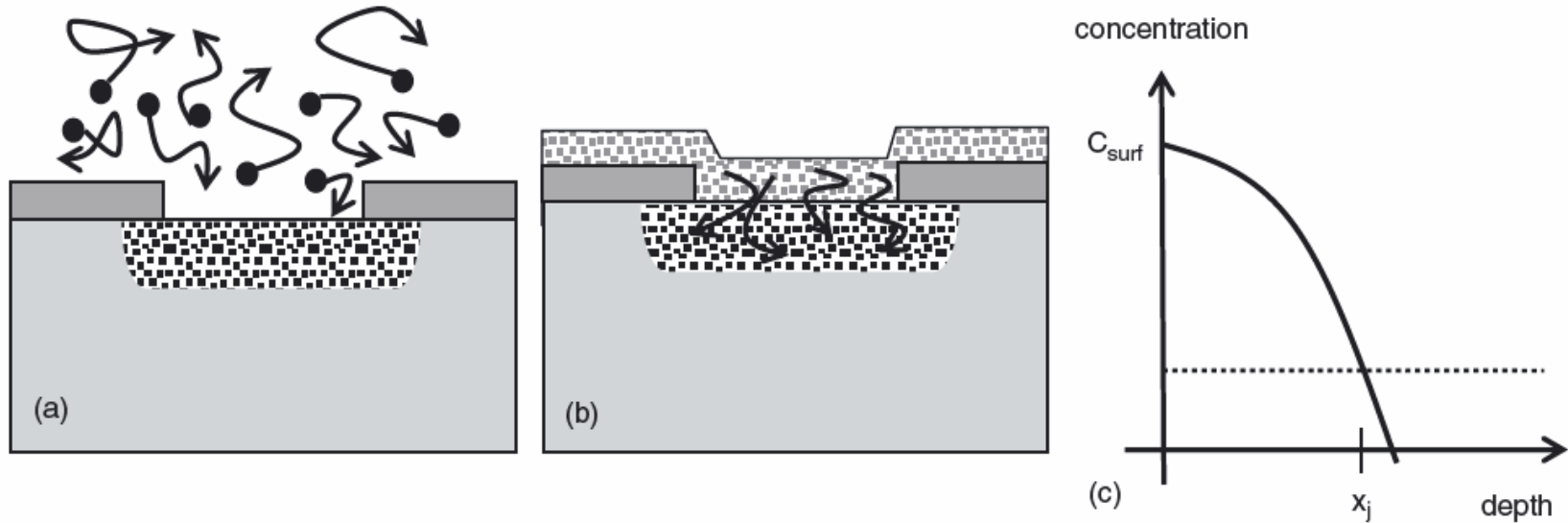
Figure 14.1 Thermal diffusion: (a) gas phase diffusion with oxide mask; (b) diffusion from doped thin film with oxide mask; (c) dopant profile and junction depth x_j

Fransila

900 – 1200 C
1000 C for 1 hour ~ 1 μm

Constant Source Diffusion

$$\frac{dC}{dt} = -D\nabla^2 C \qquad \text{Diffusion equation}$$

For a constant source concentration C_0 at the surface:

$$C(z) = C_0 \operatorname{erfc}\left(\frac{z}{2\sqrt{Dt}}\right)$$

$$\operatorname{erfc}(x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2}\, dt$$

erfc(x)

The concentration decreases about linearly

$$\operatorname{erfc}(z) = 1 - \frac{2z}{\sqrt{\pi}} + \cdots$$

Constant source diffusion

The diffusion equation is,

$$\frac{\partial C}{\partial t} = D\nabla^2 C.$$

In constant source diffusion, the concentration is held constant at the surface. The concentration of dopants is,

$$C(z,t) = C_0 \text{erfc}\left(\frac{z}{\sqrt{4Dt}}\right).$$

The concentration falls at the surface and the total number of dopants remains constant.
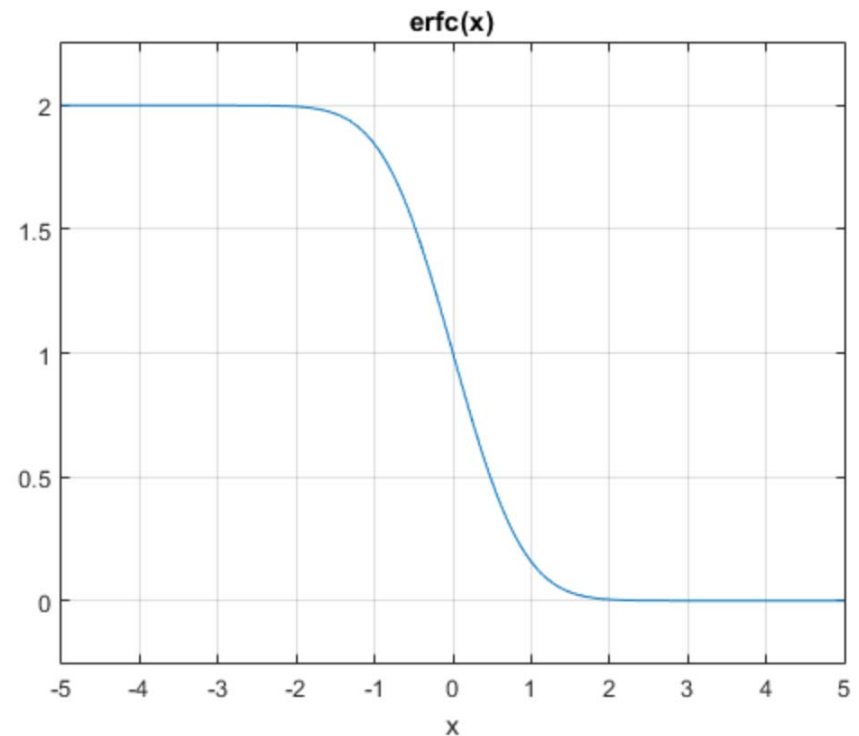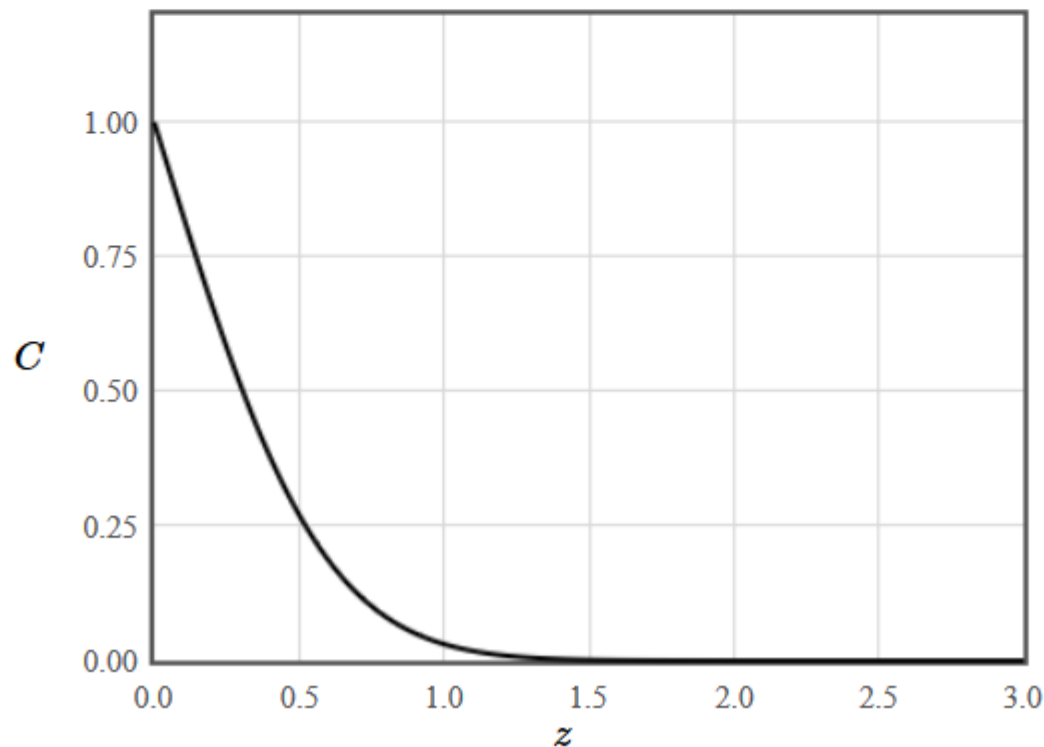

Limited Source Diffusion

$$\frac{dC}{dt} = -D\nabla^2 C$$

Diffusion equation

For a limited source concentration C_0 at the surface:

$$C(z) = \frac{C_0 w}{\sqrt{4\pi D t}} \exp\left(-\frac{z^2}{4Dt}\right)$$

$$C(z) = \frac{C_0 w}{\sqrt{4\pi D t}} \left(1 - \frac{z^2}{4Dt} + \cdots\right)$$

Limited source diffusion

The diffusion equation is,

$$\frac{\partial C}{\partial t} = D\nabla^2 C.$$

If a limited source of dopants is deposited in a thin layer with a thickness w at the surface such that the dose Q in dopants per square meter is $Q = \int_0^w dz$, the concentration as a function of time

$$C(z,t) = \frac{Q\exp\left(\frac{-z^2}{4Dt}\right)}{\sqrt{4\pi Dt}}.$$

The concentration falls at the surface and the total number of dopants remains constant.

restart
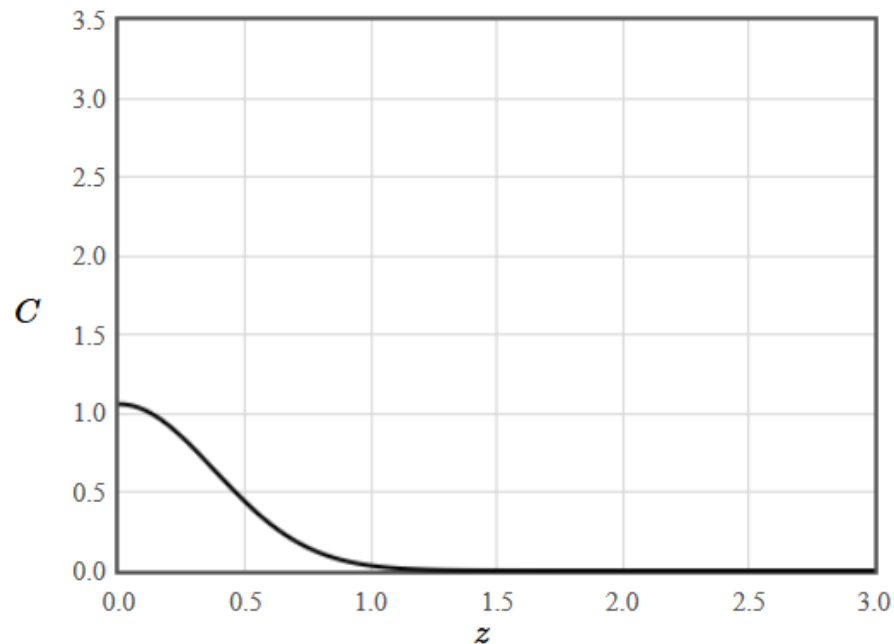
Diffusion is thermally activated
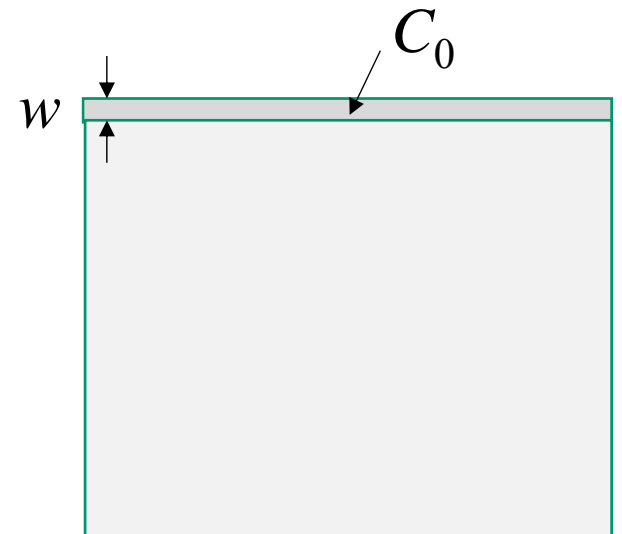
$$D = D_0 \exp\left(\frac{-E_A}{k_B T}\right)$$

$$L = \sqrt{4D_0 \exp\left(\frac{-E_A}{k_B T}\right) t} \qquad \text{Diffusion length}$$

For P diffusion, 1 h, at 1200 $T = 1473$ K

$$L = 1.3 \ \mu\text{m}$$

	Si	B	In	As	Sb	P	Units
D_0	560	1.0	1.2	9.17	4.58	4.70	cm^2 sec^{-1}
E_A	4.76	3.5	3.5	3.99	3.88	3.68	eV

Diffusion

Interstitials and vacancies diffuse quickly and assist the dopants.

BH_3 diffuses faster than B.

Diffusion depends on doping concentration.
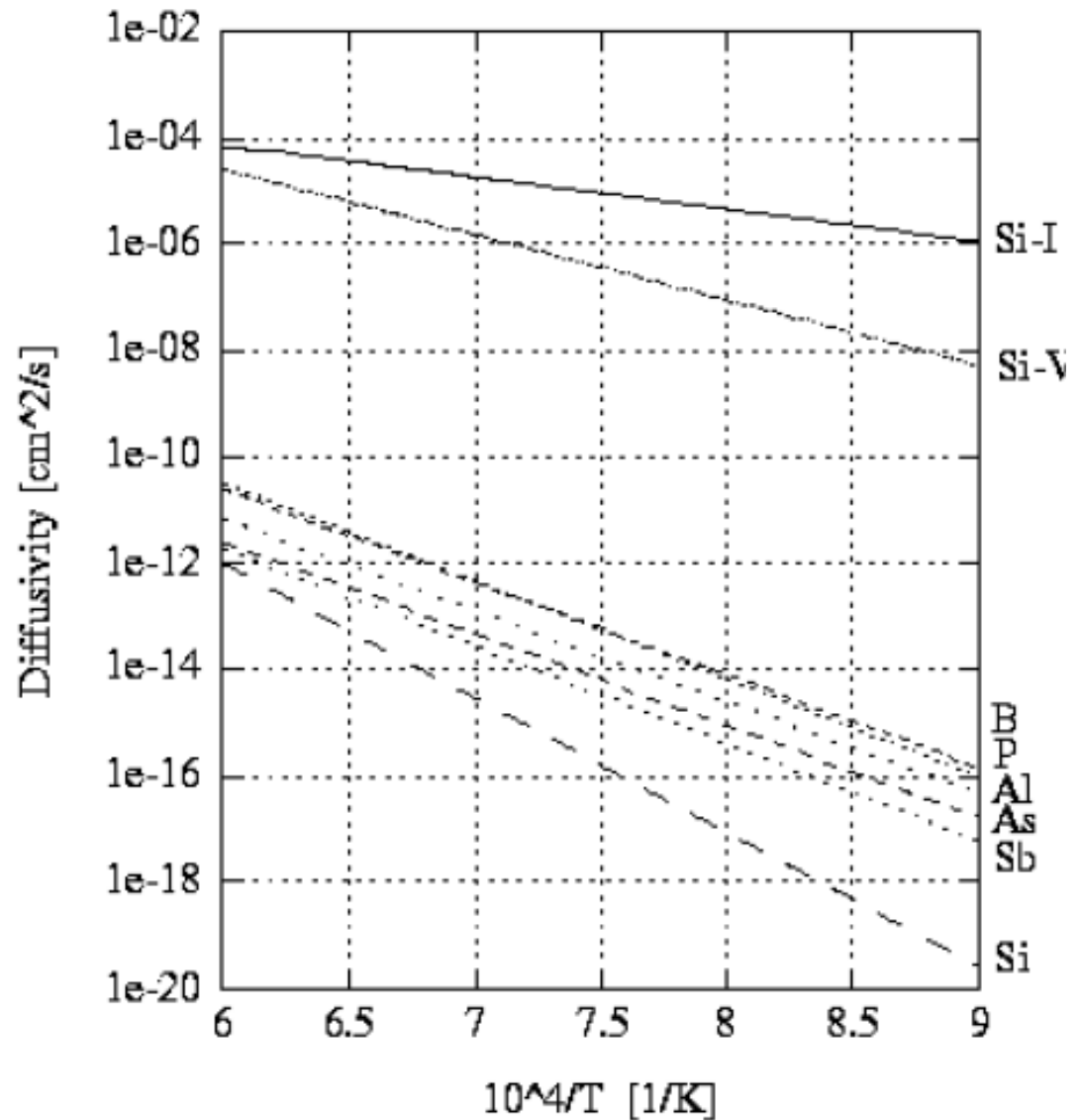
Solid solubility limits

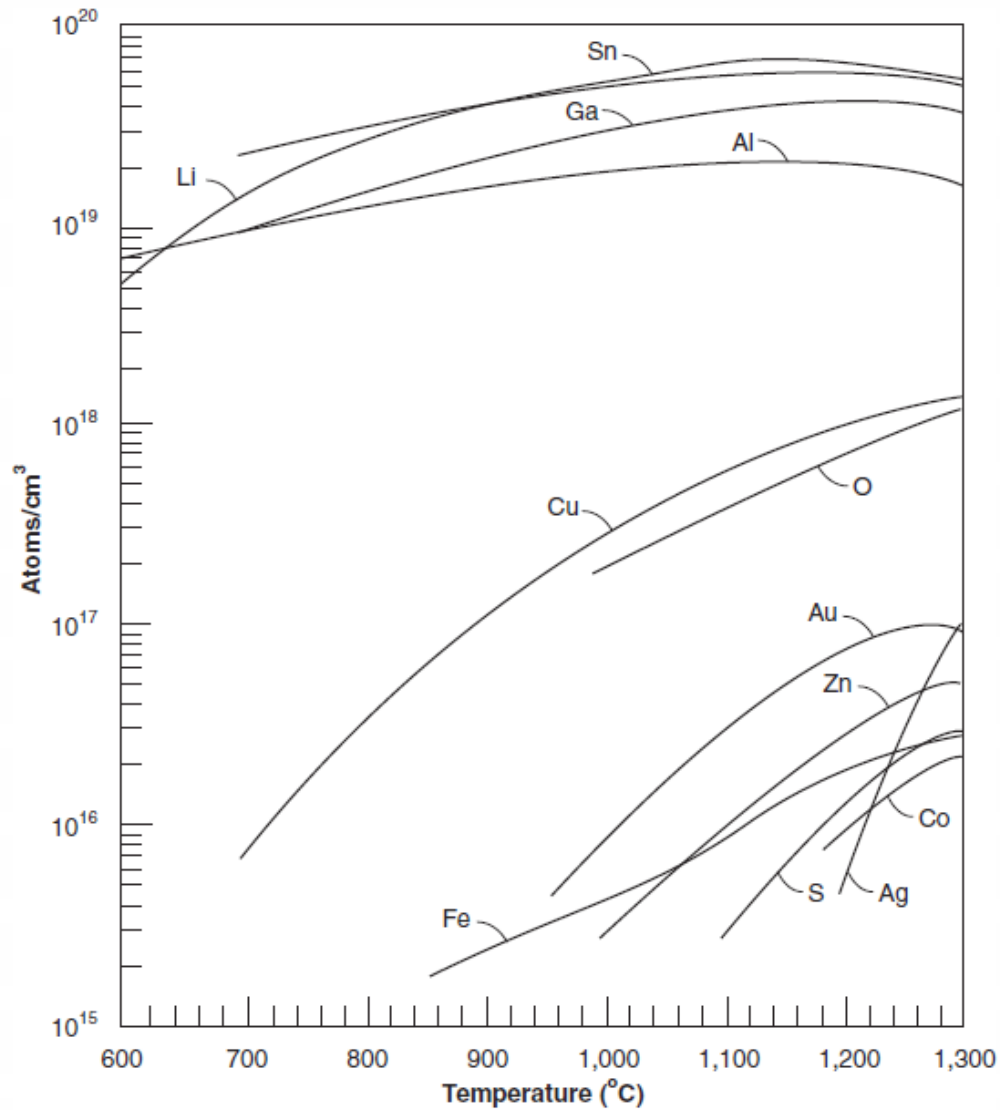Figure 1.28: Solid solubility of selected impurities in silicon [47].

Predeposition/Drive-in

Oxide diffusion mask ~ 500 nm

Predeposition process
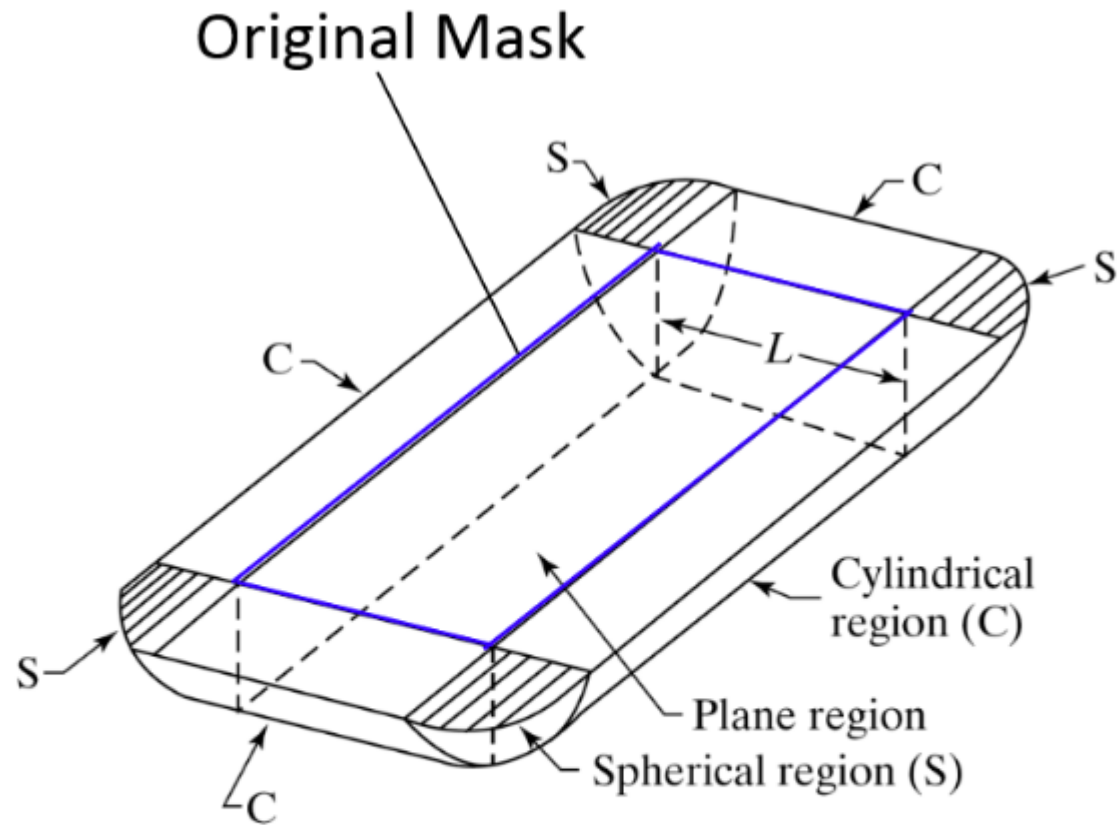   spin-on glass
      ion implantation
      constant source diffusion

Drive-in process
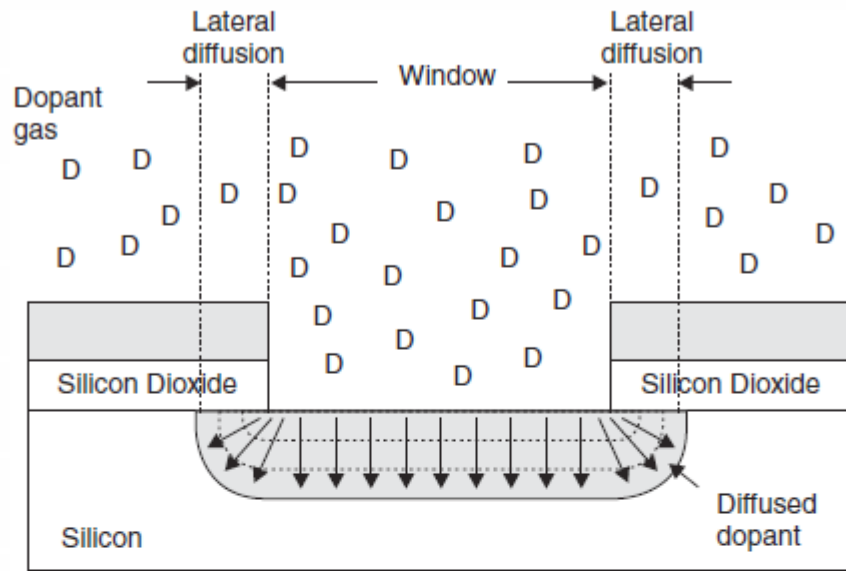   limited source diffusion

Patterned dopant regions

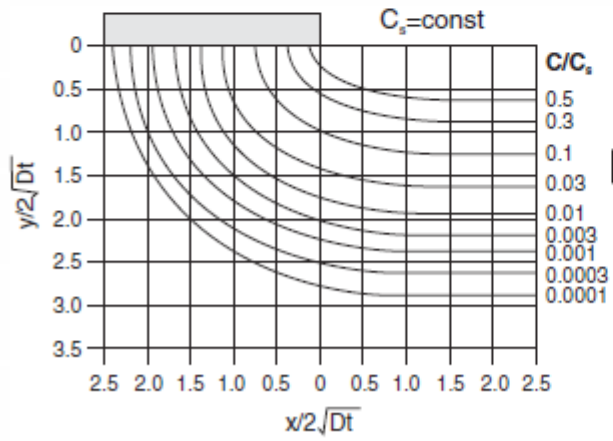**Figure 1.34: Pre-deposition through a silicon dioxide window.**

a) Complementary error function
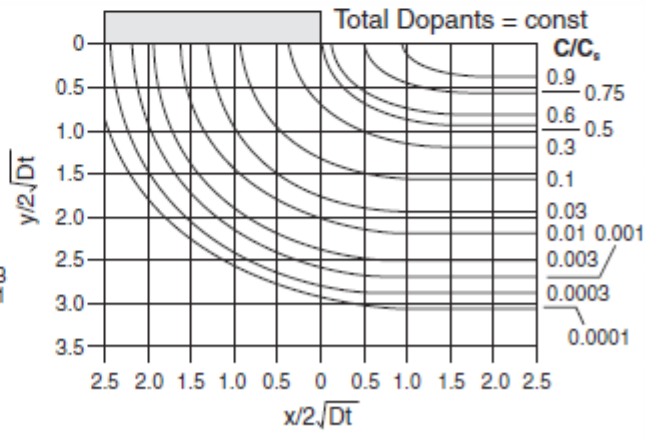
b) Gaussian

Ion implantation

substrate

separation magnet

U_{decell}

U_{accell}

A

current integrator

ion source
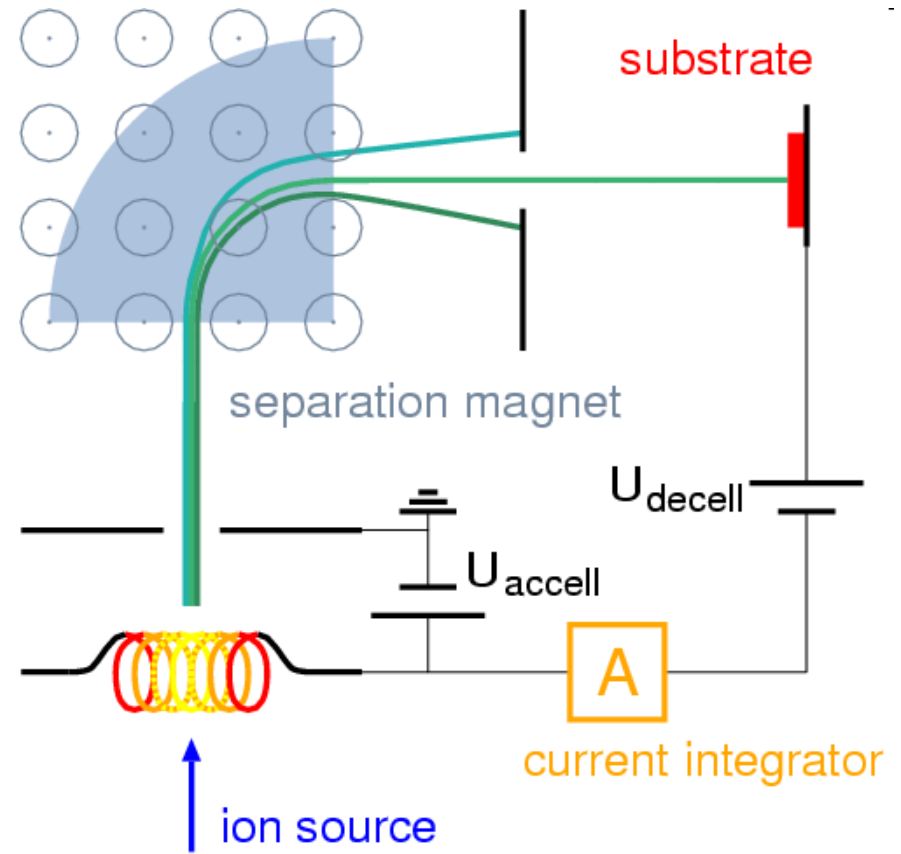
X-rays are generated

Ion implantation

More accurate control of concentration

Better lateral confinement

Low temperature

Complex profiles through multiple implantations

Less sensitive to surface preparation

Requires an anneal to eliminate damage and activate dopants

Dopants diffuse during the anneal

Possible to implant above the solubility limit

http://slideplayer.com/slide/2412041/
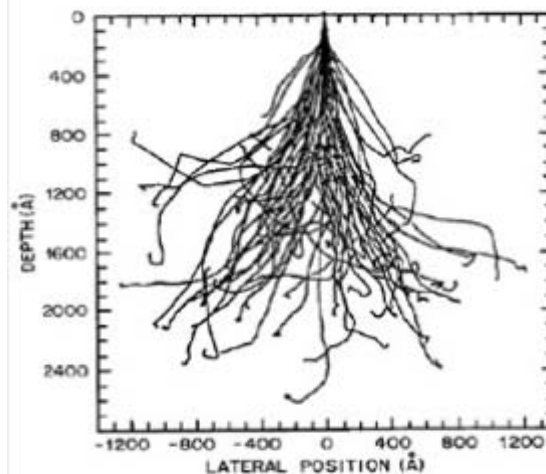
Ion implantation

Photoresist, oxide, or nitride. Should be thicker than projected range. High doses burn the photoresist on and make it hard to remove.
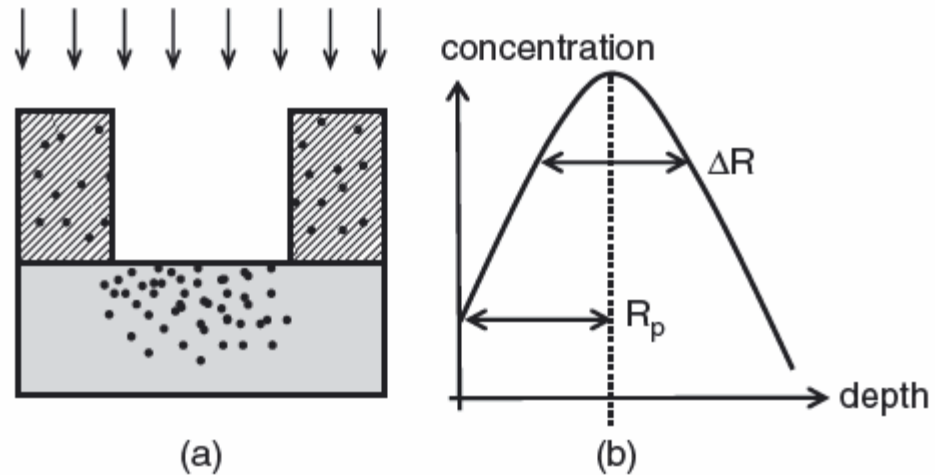
Figure 15.1 (a) Implantation: mask layer blocks selected areas; (b) dopant concentration profile inside silicon, with projected range R_p and straggle ΔR

Most dopants are at the projected range R_p.

Ion implantation
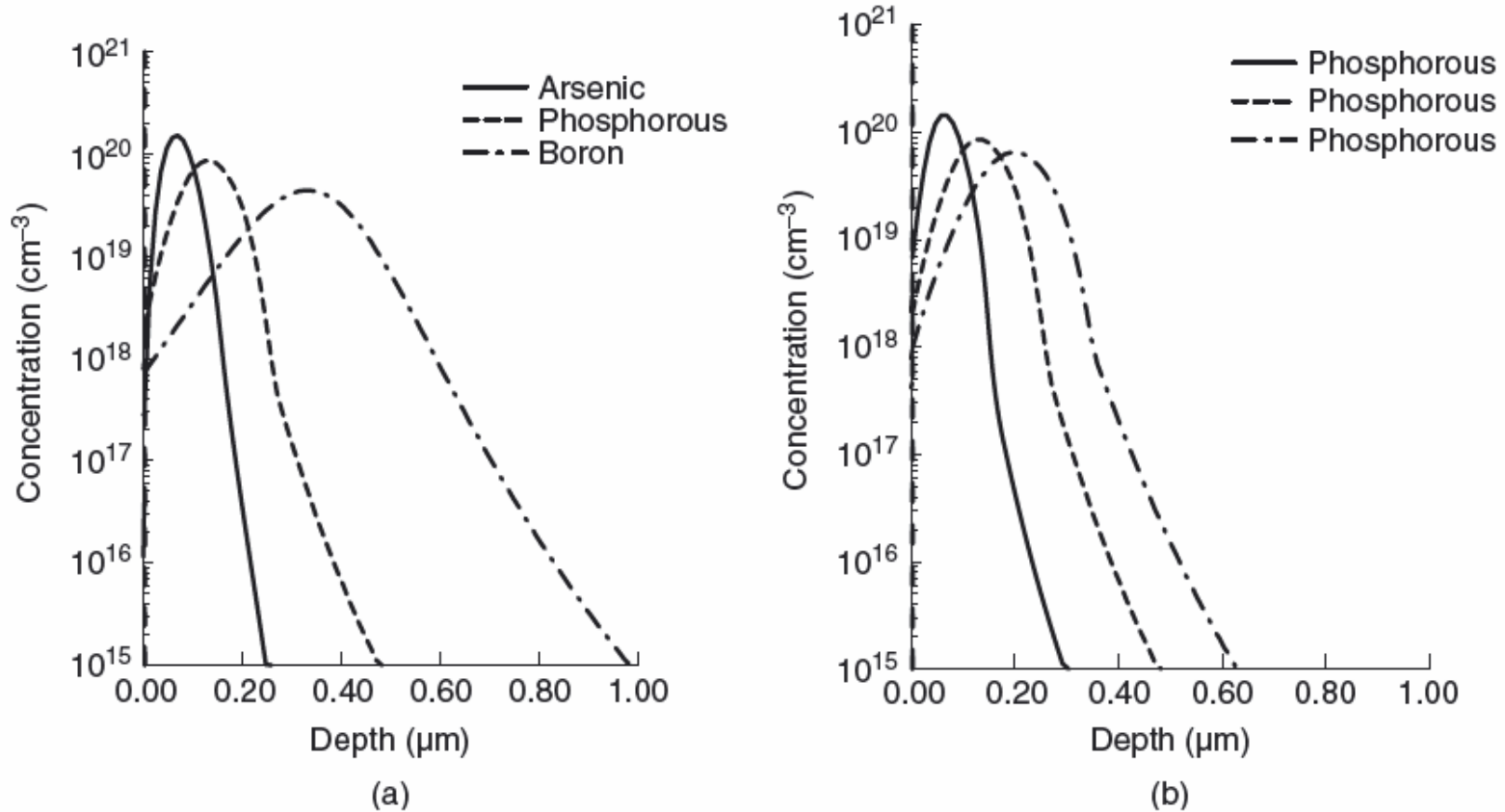
Figure 15.3 (a) The 50 keV implantation of arsenic, phosphorus and boron: the lighter ions will penetrate deeper. (b) Phosphorus implantation with 50, 100 and 150 keV energies

SRIM
The Stopping and Range of Ions in Matter

James F. Ziegler, Jochen P. Biersack, Matthias D. Ziegler

SRIM

The Stopping and Range of Ions in Matter

J. F. Ziegler
J. P. Biersack
M. D. Ziegler
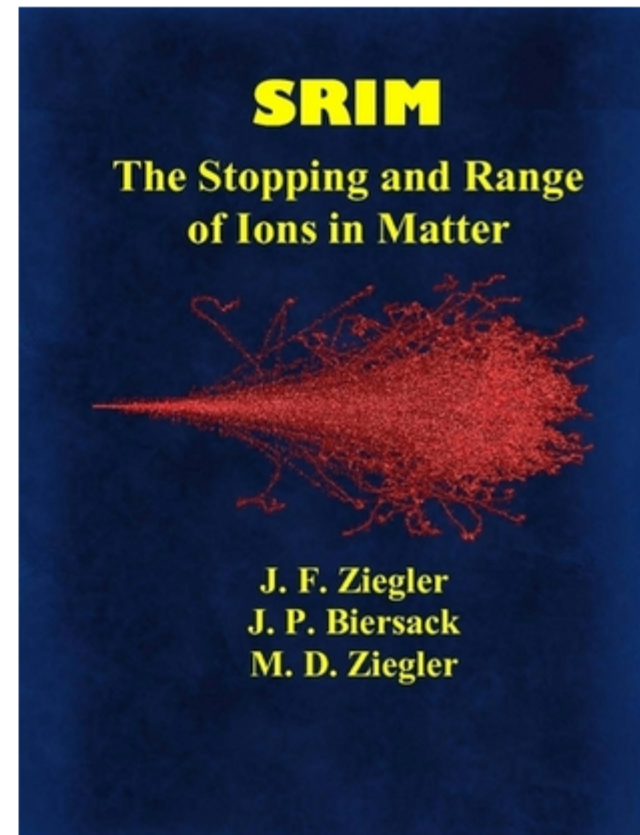
Rapid thermal anneal (RTA)

http://www.appliedmaterials.com/products/vantage-radianceplus-rtp
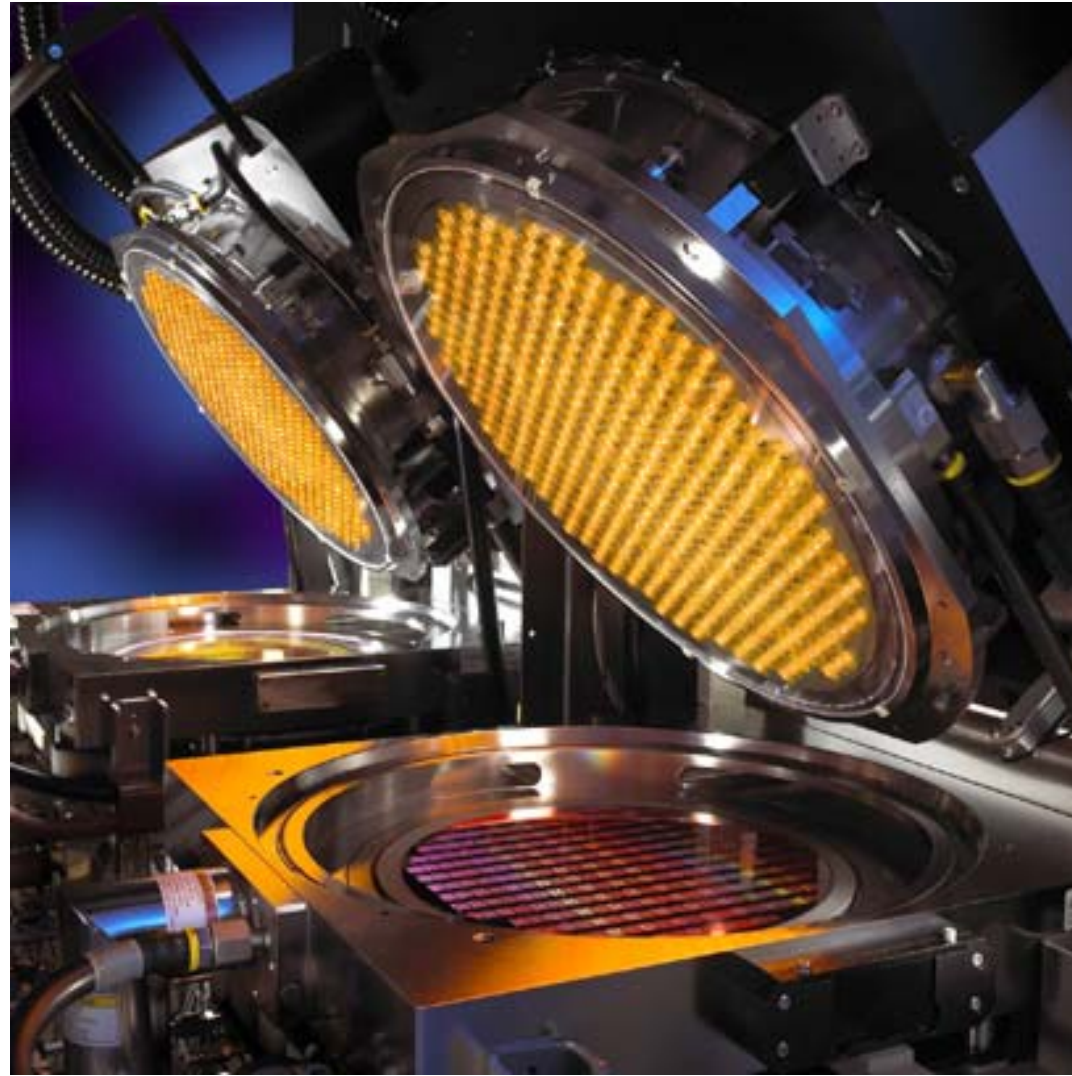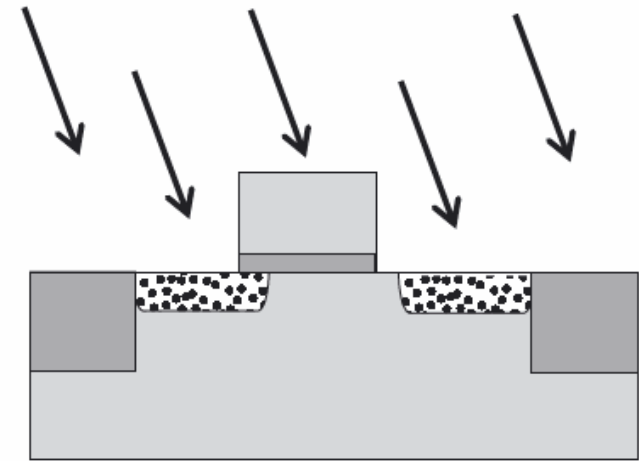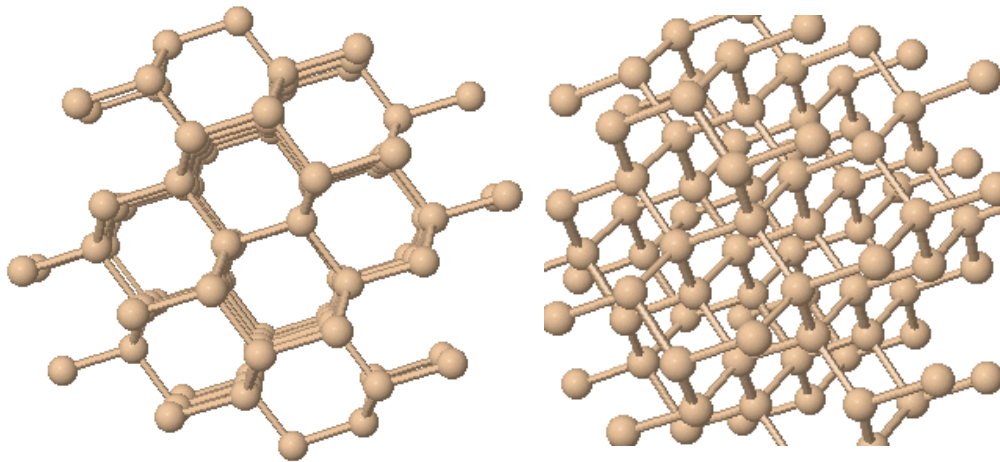
Channeling

Figure 15.6 Doping asymmetry due to tilted implantation

Ions travel deep into the crystal when the beam is aligned with a crystal axis. Implantation is often done at 7° off-axis to avoid channeling.
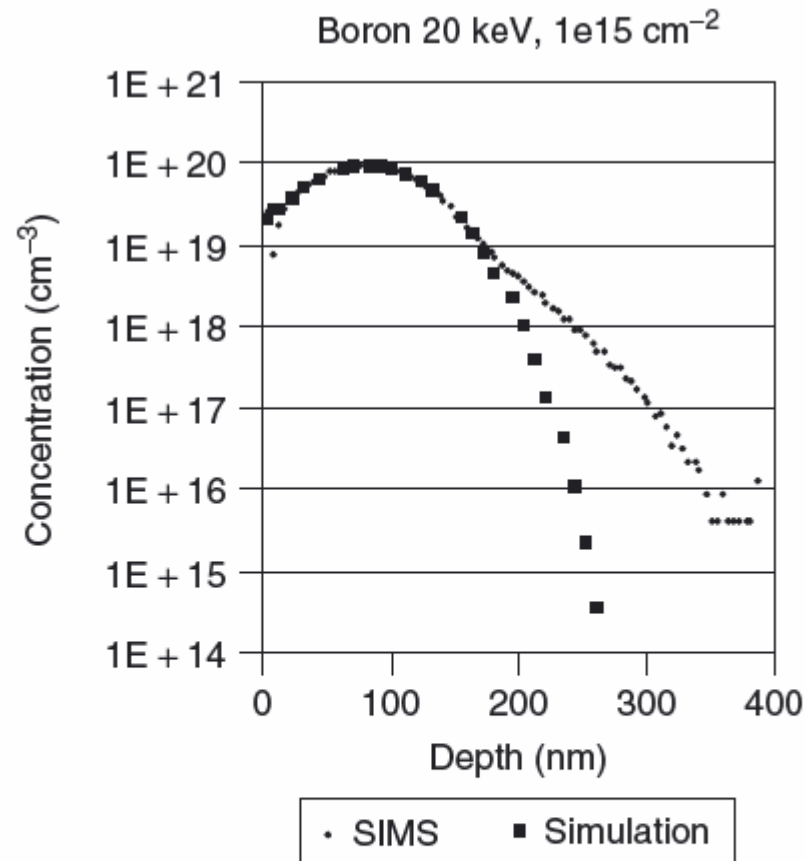
Figure 15.9 Boron implantation into silicon, 20 keV, 10^{15} cm^{-2}. SIMS measured data shown by small diamonds, ICECREM simulation by large squares. The discrepancy in the tail results partly from ion channeling and partly from model deficiencies. SIMS data courtesy Jari Likonen, VTT

Plasma immersion ion implantation

PLASMA IMMERSION ION IMPLANTATION PRINCIPLES

External source and pulsed mode:

- Limitation of plasma/surface interactions
- Low contamination level
- Wide range of plasma density
- Limitation of wafer charging

ON
OFF

Plasma source

Plasma

O
-HT
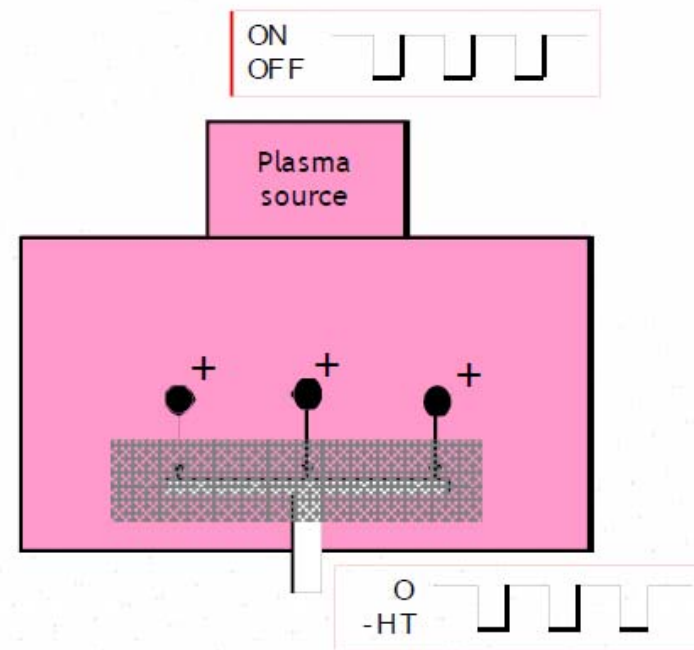
Flat panel displays and solar panels.

Oxidation

The properties of SiO_2 were more important than Si in making Si the dominant semiconductor material.

Thin gate oxide ~ 1 nm in MOSFETs
Tunnel barriers in flash memory
Dielectrics in capacitors
Electrical isolation of components
Passivation layer to protect the circuits
Oxide masks for diffusion and implantation

Native oxide ~ 1 nm grows in air in hours but is not good quality

Thermal oxide - grows slowly, best quality

Deposited oxide - grows quicker, less quality

Dry oxidation

$$Si\ (s) + O_2\ (g) \rightarrow SiO_2\ (s)$$

1 hour at 900 C produces 30 nm of thermal oxide.

Used for gate oxide in MOSFETs and tunnel oxide flash memories.

Good layer control. Low defect density at the Si/SiO_2 interface.

Wet oxidation

$$Si\ (s) + 2H_2O\ (g) \rightarrow SiO_2\ (s) + 2H_2\ (g)$$
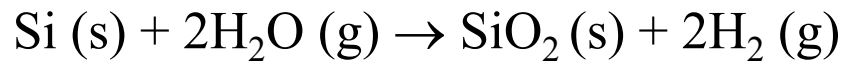
The water is steam.

1 hour at 900 C produces 130 nm of thermal oxide.

Faster growth than dry oxidation.

Quartz Oxidation Tube

Steam

Steam Chamber

Torch

H₂

O₂

Torch Element

Furnace Element

The External Torch
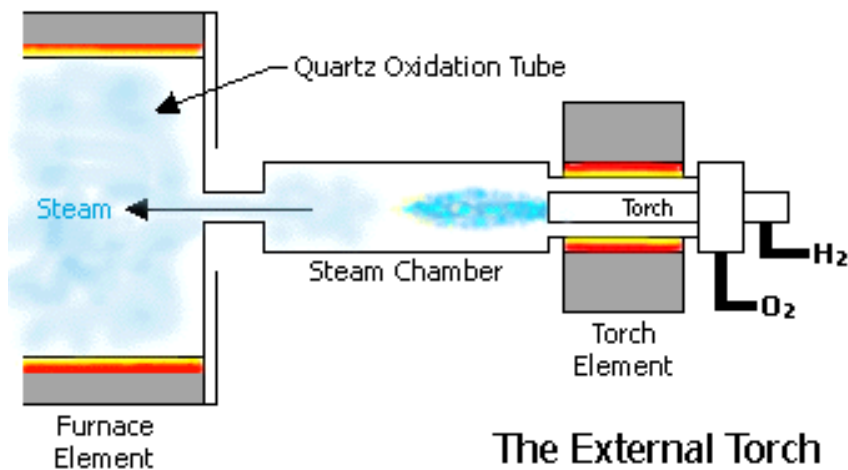
CVD oxides

Can be deposited at lower temperature

Rougher surfaces, lower breakdown field, higher etch rate in HF

Deal-Grove oxidation model

Oxide thickness z is first linear then grows like a square root
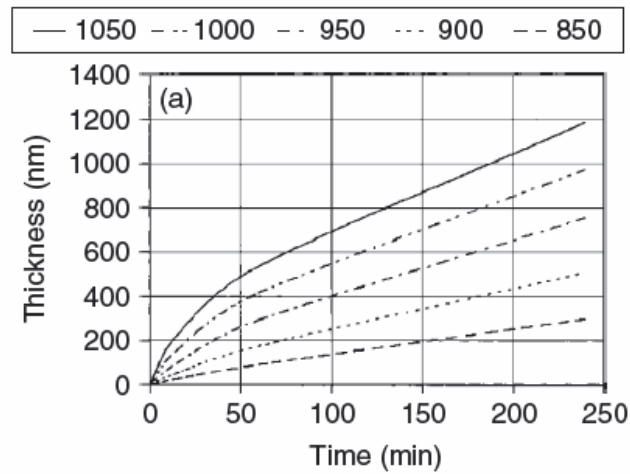
$$z(t) = \frac{-A + \sqrt{A^2 + 4Bt}}{2}$$

The constants are thermally activated

$$B = B_0 \exp\left(\frac{-E_A}{k_B T}\right) \qquad \frac{B}{A} = \left(\frac{B}{A}\right)_0 \exp\left(\frac{-E_A}{k_B T}\right)$$

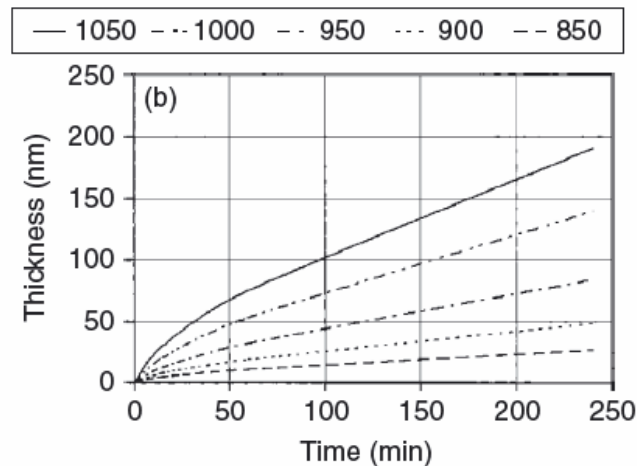| Parameter	Quantity		Wet (H_2O)	Dry (O_2)
Linear rate constant	$(B/A)_0 \left(\frac{\mu m}{hr}\right)$		<100>: 9.7×10^7 <111>: 1.63×10^8	<100>: 3.71×10^6 <111>: 6.23×10^6
	E_A (eV)		2.05	2.00
Parabolic rate constant	$B_0 \left(\frac{(\mu m)^2}{hr}\right)$		386	772
	E_A (eV)		0.78	1.23

Deal-Grove oxidation model

Wet

Dry

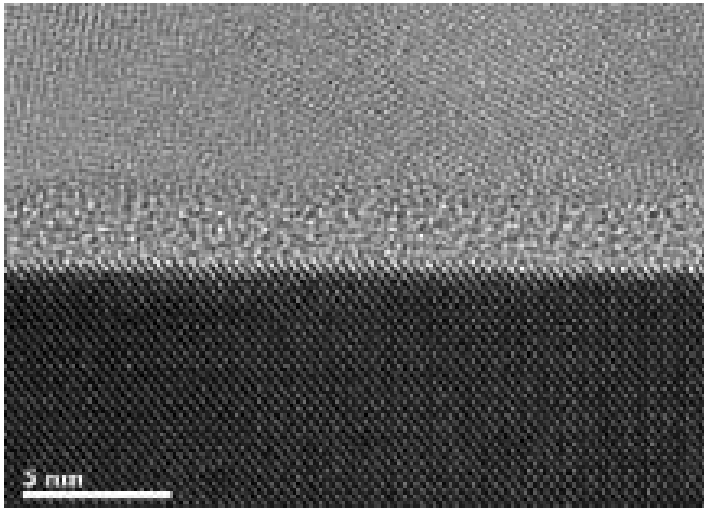Linear dependence: Limited by the reaction rate of Si and O_2 to SiO_2

Square root behavior: Limited by oxygen diffusion through the oxide.

Figure 13.3 Oxidation of <100> silicon at temperature between 850 and 1050°C, wet and dry. Maximum prac tical oxide thickness is 1 or 2 micrometers, because of th decrease in parabolic oxidation rate
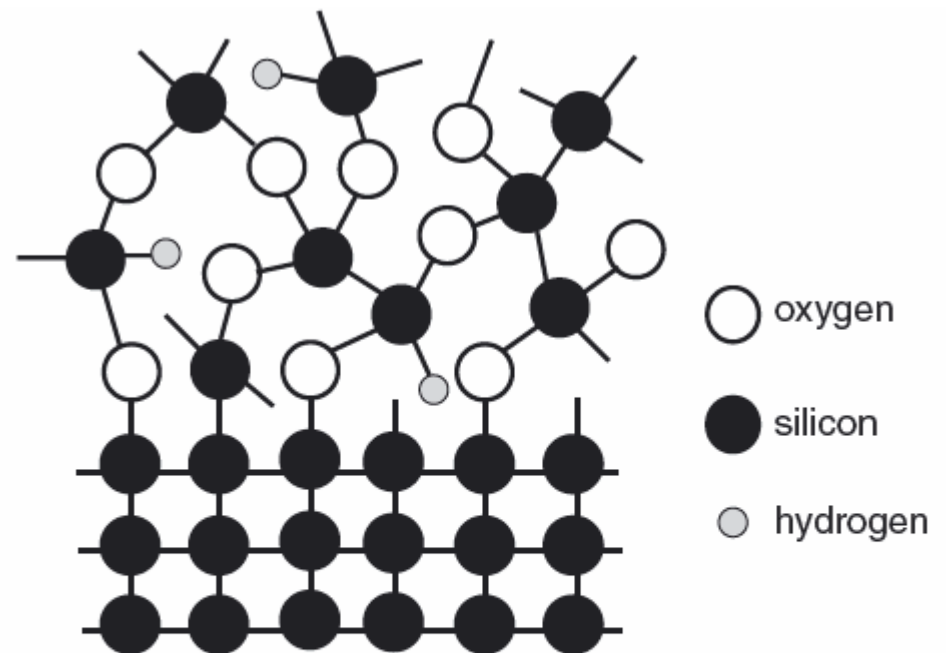
SiO$_2$ is amorphous

gate oxide

Post oxidation anneal (N$_2$ then H$_2$) to passivate dangling bonds

http://www.nanolabtechnologies.com/

D_{it} 10^9–10^{11}/cm^2
defects at the interface

10^{15} atoms/cm^2

oxygen

silicon

hydrogen

Figure 13.8 The structure of the silicon/silicon dioxide interface: single crystalline silicon and amorphous oxide. There are dangling bonds (not having their full valence) and some have hydrogen atoms bonded to them

Fransila

Oxides are under compressive stress

Typical stress is 300 MPa
Stress will bow the wafer
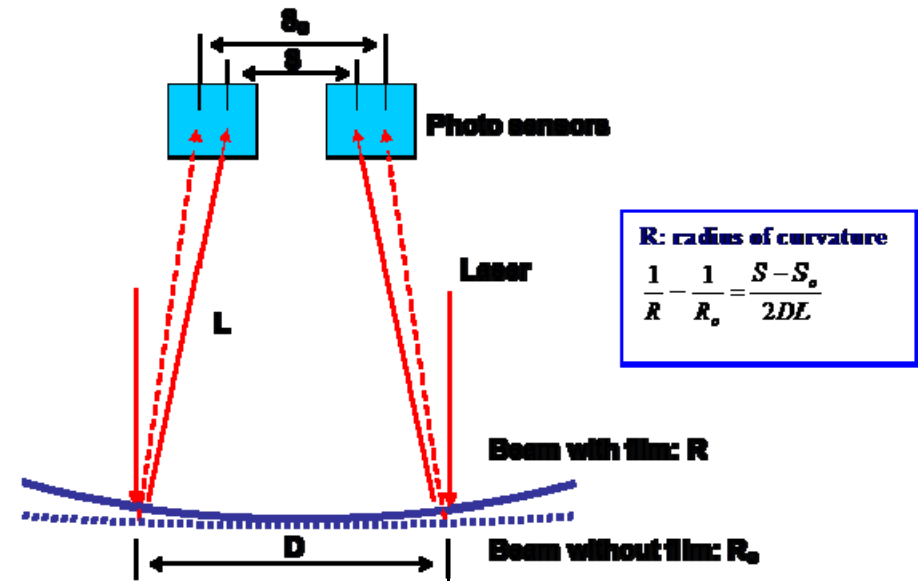
density
quartz 2.65 g/cm^3
oxide 2.2 g/cm^3

Young's modulus
quartz 107 GPa
oxide 87 GPa

Stoney's formula

$$\sigma_f = \frac{E_s h_s^2 \kappa}{6 h_f (1 - v_s)}$$

R: radius of curvature
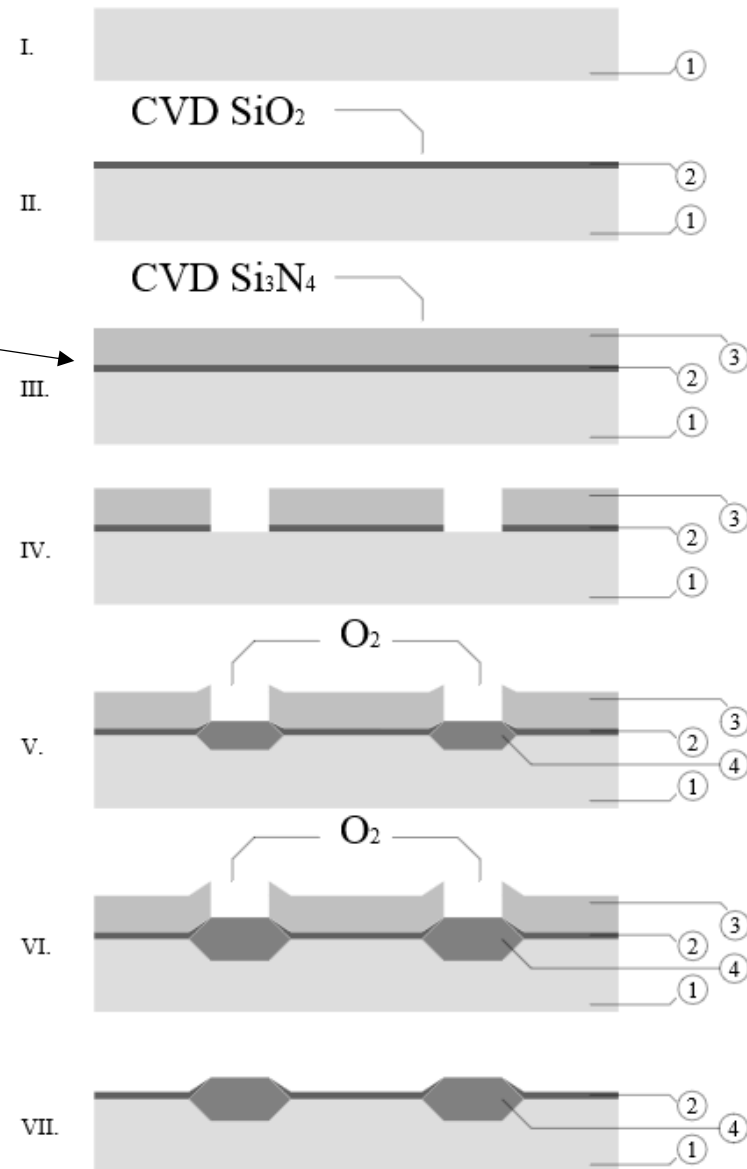
$$\frac{1}{R} - \frac{1}{R_o} = \frac{S - S_o}{2DL}$$

The stress σ_f in the film depends on
E_s Young's modulus in the substrate
v_s Poisson's ratio of the substrate
h_s thickness of the substrate
h_f thickness of the film
κ curvature

Only holds for uniform curvature

Local Oxidation of Silicon (LOCOS)
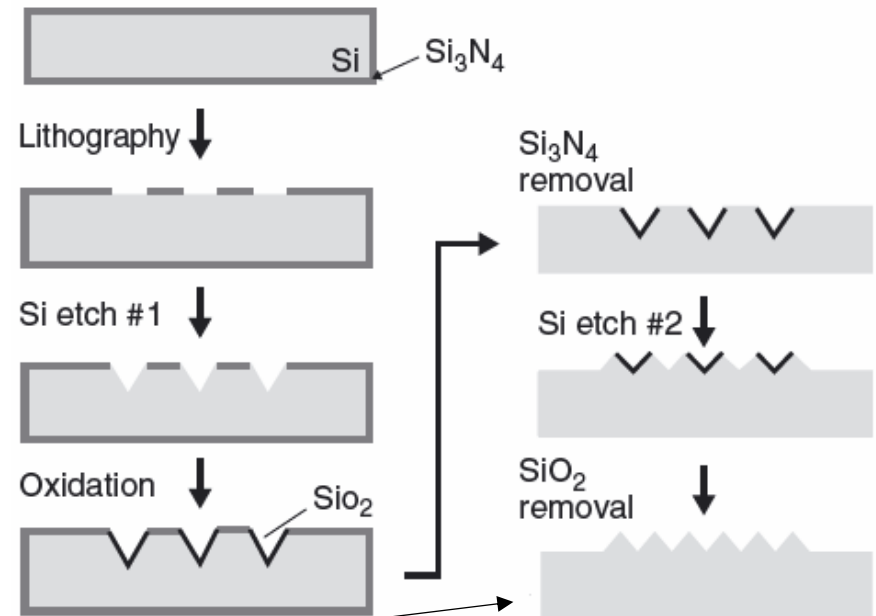
thin pad oxide for stress relief

Controlled removal of Si

1. Thermal oxidation (good control of thickness)

2. Etch Oxide with HF

Period doubling of pattern

Figure 13.10 LOCOS for a sawtooth structure in (100) silicon. Nitride first acts as a silicon etching mask and then as an oxidation mask. Second KOH etching and HF oxide removal result in sawtooth relief. Reproduced from Ribbing *et al.* (2003), copyright IOP

Controlled removal of Si
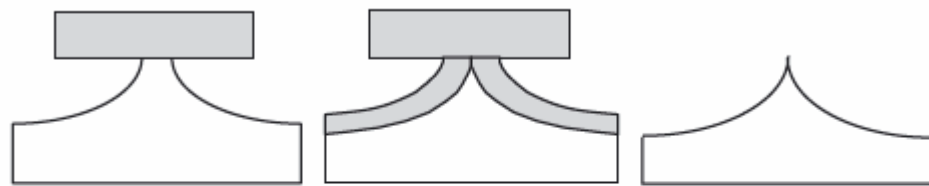
Figure 13.14 Silicon tip fabrication: left, isotropic silicon etching with an oxide mask; middle, thermal oxidation; right, silicon tip recovery by HF etching
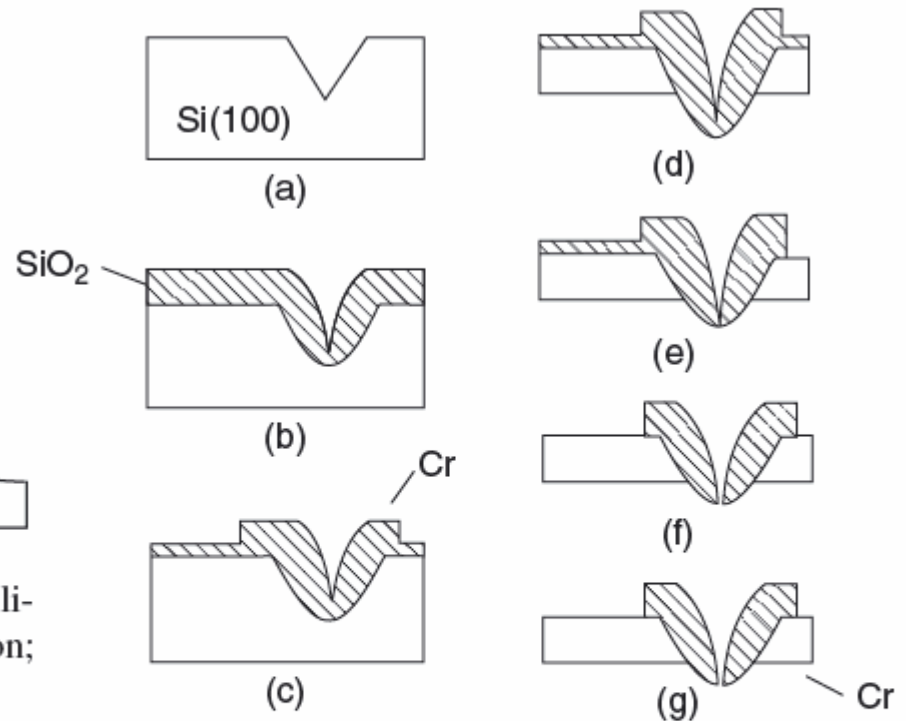
Figure 13.13 Oxide thinning at the apex is used as a method to fabricate nanoscopic holes: the apex can be etched open while leaving oxide elsewhere because oxide is thin and stressed at the apex. Reproduced from Minh and Ono (1999) by permission of AIP

Fransila

Complementary Metal Oxide Semiconductor (CMOS)

The dominant technology for microprocessors

Low power dissipation through the use of n-type and p-type MOSFETs